The Engineer's Computer

RAYTHEON 250 DIGITAL COMPUTER

The advent of small, low-cost engineering and scientific computers has given the engineer a new tool. Although larger digital computers have played an important role in research and design, the cost has limited their use to the most extensive problems. Because of this, most engineers continue to solve many problems with slide rule and desk calculator. Using the small computer, the individual engineer has direct access to analyze the problem, program the computer and tabulate the answers.

The engineer with a problem to be solved on a digital computer no longer finds it necessary to explain the problem to the programmer, arrange to have machine time available and then wait for the results. Large computers require maximum use by skilled programmers to amortize their cost. The relatively inexpensive small computer can be immediately available to the engineer and adjacent to his desk. The engineer can be trained to use the computer effectively in a few hours. With experience, he will learn to use the computer to minimize manual computations and, ultimately, to reduce overall engineering time.

Minor errors no longer cause long delays. Program or computational errors may be ascertained quickly and corrected by observing the operation of the machine. Because the engineer is included in the computation loop, his ingenuity and experience may be used to aid the problem solution. The engineer may observe trends in the results, stop the program and rearrange data at will.

The small computer is not intended to replace larger ones, but in fact complements them. They may be used to solve problems that are not economical to program on the large machines. Small computers also may be used in conjunction with large computers. They can check out portions of large programs to evaluate programming techniques, ascertain the most economical programming methods as well as estimate the amount of time necessary to execute programs on large machines.

The use of small digital computers is ideally suited for design problems where repetitive or extensive calculations are necessary. The small computer is ideal in circuit, filter and worst-case design. The computers best lend themselves to applications where an engineer using a slide rule or calculator can solve the problem in several hours. With the small computer, the engineer can have a solution in a few minutes.

COMPUTER HARDWARE

Basically all digital computers have four functional parts. These parts are: input/output devices, a memory, an arithmetic section and a control section.

Through the input/output devices, the computer receives instructions and data and provides the answers that it produces. Computer instructions and data may be entered with a manual device: a typewriter or a separate keyboard having special designations. Magnetic tape, punched cards and punched tape are used for a more rapid entry. The method used is dictated by the ultimate use of the computer and often these devices are used to increase the memory of the computer. Cards and magnetic tape offer a convenient method of up-dating permanent storage. Paper tape is more convenient to use with the small computer, although most computers have parallel input channels available for use with more than one type of input equipment.

New price — $23,500 We give you 3856 words for $23,500

	Model	Monthly rental (dollars)	Outright sale (dollars)	Compatible auxiliary equipment	Memory type	Memory storage (words)	Word size (bits)	Software available I = Interpreter C = Compiler A = Assembler	Program system used	Programming time	Execution time per solution
Burroughs Corp. Second Ave. at Burroughs Detroit 32, Mich.	E103	900	28,400	Card Magnetic tape	Drum	220	Variable serial	None	Machine language	16 to 24 hr	60 sec
Control Data Corp. 8100 34th Ave. S. Minneapolis, Minn.	G15D	995 to 1530	22,500	Card Magnetic tape Graph plotter	Drum	2176	29	I, C, A	INTERCOM 500	0.5 hr	45 sec
	8090 control computer	Not available	45,500	Card Magnetic tape Graph plotter Line printer	Core	4096 expandable	12	I, C, A	FORTRAN	0.25 hr	12 sec
Digital Equipment Corp. Maynard, Mass.	PDP-5	900	27,000	Card Magnetic tape CRT display	Core	4096 expandable	12	I, C, A	FORTRAN 2	Variable	9 sec
General Precision, Inc. Commercial Computer Div. 101 E. Tujunga Ave. Burbank, Calif.	LGP21	Not available	21,500	Card Teletype	Disc	4096	32	I, C	Floating Pt. interpreter	0.5 hr	50 sec
	LGP30	1100	24,500	Card	Drum	4096	32	I, C, A	Floating Pt. interpreter	0.5 hr	17 sec
	RPC4000	1865	47,000	Card	Drum	8008	32	I, C, A	Floating Pt. interpreter	0.5 hr	5 sec
Pacific Data Systems 1058 E. First St. Santa Ana, Calif.	PDS1020	Variable	21,500	Parallel input/output channels for use with other manufacturers' equipment	Delay line	2048 expandable	17	I, A	Engineering interpreter	0.3 hr	30 sec
Packard Bell Computer 2700 S. Fairview Santa Ana, Calif.	PB250R-4	1300	33,300	Card Magnetic tape Recorder Data systems	Delay line	2320 expandable	21	I, C, A	CINCH	Less than 1 hr	1 sec
Scientific Data System 1649 17th St. Santa Monica, Calif.	SDS910	1740	51,000	Card Magnetic tape CRT display Line printer Graph plotter	Core	2048 expandable	24	C, A	FORTRAN 2	Less than 1 hr	4 sec

We're now Raytheon!

Look page

TO *give the design engineer an indication of the availability and variety of small computers, EDN has surveyed the computer market and prepared this table.*

In listing the manufacturers, EDN placed a maximum limit of approximately $50,000 for outright sale.

EDN established minimum input/output devices to insure versatility. To enter variable data, a manual input device was required. In most machines, manual entry is made with an electric typewriter although a separate keyboard is used sometimes. Printed output also was required. All computers listed use an electric typewriter. Rapid entry of pre-prepared data or information precludes entering data manually. EDN required that one method of automatic information entry and retrieval be included in basic cost of computer. Output device was required to prepare and store data in a format suitable for re-entry in the computer. All computers listed use punched paper tape. Information is entered into the computer by a paper-tape punch and reader as a separate device or by units associated with the electric typewriter. It is with these devices that the software programs or pre-prepared data are entered. Using tape, a program can be prepared, used and then stored to eliminate duplication of effort when similar problems are encountered.

The chart lists some of the basic types of software used with these computers. Interpreter programs convert mathematical language into machine language. Often included in interpreters are subroutines that will perform square root, power and trigonometric functions with a single command. Interpreters generally create machine language to be used directly in a sequence of instructions in machine language. The assembler is a utility program that uses symbolic address notation in place of the machine-language addresses. A compiler is a programming system that accepts problem statements in a problem-oriented language and converts these statements to a language suitable for direct machine processing.

To give the design engineer an indication of the time required to solve problems using the digital computer, each manufacturer was asked to solve the RLC problem given in the example. Absolute values of impedance and phase angle were requested for 10 values of ω with component values held constant. The programming time typically varies with the individual, but only seconds were required to execute the calculations and print answers.

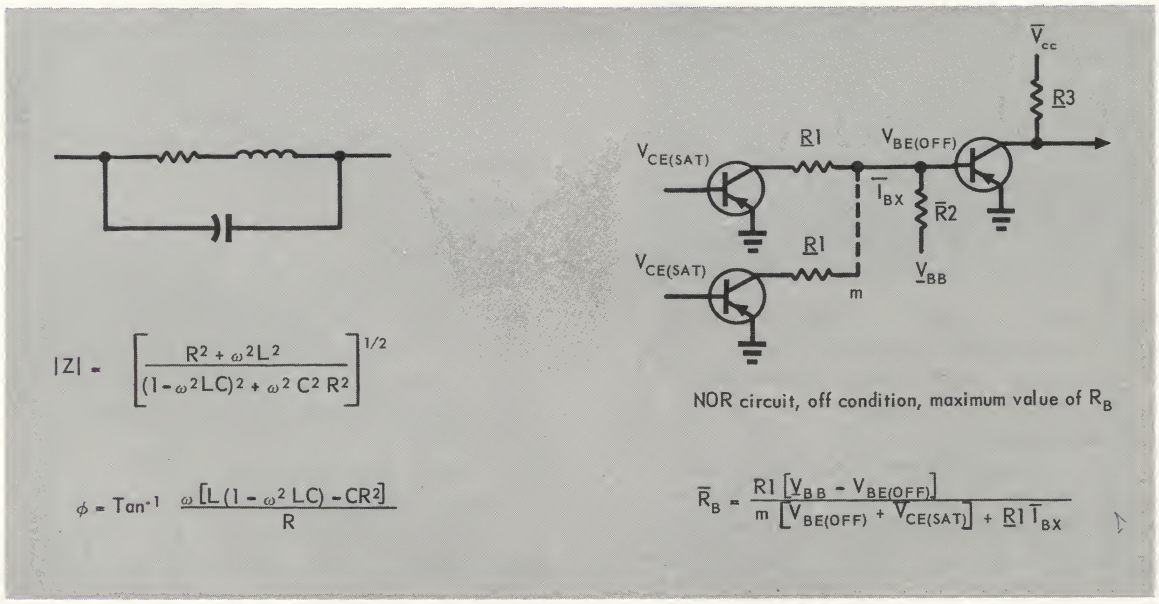
We now have Fortran II to speed up and simplify programming!

For printed output, the low-cost computer normally uses a typewriter and has some method of punching paper tape for a stored output. As with the input devices, many of the computers are compatible with other output devices such as card punches, magnetic tape, line printers, chart plotters and CRT display. The significant trade off is system complexity versus ease of use: the more complex the equipment, the further its engineer is removed from the computation loop.

The computer memory is used to store the instructions as well as data on which it operates. There are several types of computer memories available that vary in speed, size and cost. Four basic types of memory are used: drum, disc, delay line and core. The compromise is memory cost versus memory speed. The fastest and highest priced device is the core memory. Core memory has complete random access so that it requires no special programming to achieve maximum retrieval time. Also, the core has nonvolatile storage and information is not lost because of power failure. The high cost of the core memory results from the relatively complex system necessary to store and retrieve information.

On the other end of the scale, the slowest memory is the rotating magnetic drum. The rotating disc memory is slightly faster but the maximum storage is usually less than that of the drum. Because the read/write heads are located at fixed points around the rotating unit, special programming techniques are necessary to achieve maximum efficiency from the computer. In low-cost computers, this is not of great importance and inefficient programming will make only a few seconds difference in the computation time of most problems.

The delay-line memory is faster than the disc or drum memories and it is slower than the core memory. Recent advancements in delay-line technology have developed it into a reliable, low-cost memory system that is used in the several low-cost computers. It is, however, a volatile system. That is, information stored in the memory will be lost if power failure occurs. In practice, the problems of memory vol-

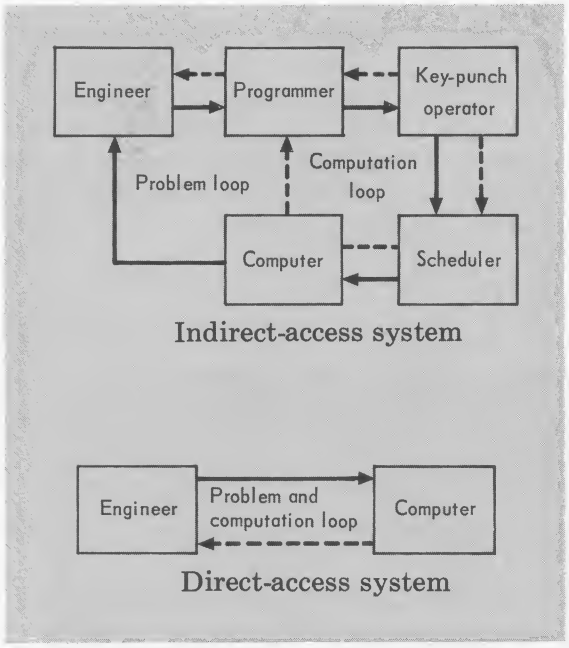


TYPICAL EXAMPLES *of problems that lend themselves to solution with low-cost digital computers. RLC circuit was used to obtain computation times shown in chart. Value of impedance and phase angle for 10 values of ω, passive components held constant, required only a few seconds after initial programming was done. Depending on the software available, solution involves a direct mathematical approach that is accomplished by setting up the basic equation of one value of ω. Multiple solutions are obtained by indexing the value of ω.*

A worst-case design may be accomplished easily on the small computer. In this case, a mathematical parallel to the breadboard treatment would be used. The equation would be set up to assign a maximum value for R_B. Parameters would be varied either in sets or for individual values to indicate the worst case.

atility are circumvented by supplying reserve power. A second method is to program the information stored in the memory on some permanent medium such as punched tape. Thus, when the information stored in the memory is lost, the computer may be programmed to reenter the information on the tape.

The arithmetic section of the computer consists of hardware that enables the computer to perform all necessary calculations. The control section or logic element of the computer coordinates the activities of the memory, input/output devices and of the arithmetic section. The complexity and cost of these sections are dictated by the input/output devices and the memory used.



SIMPLE FLOW CHART *graphically illustrates some of the advantages of the small computer. Solid lines indicate flow of information between elements in a large computer system. Dashed lines indicate the path followed when errors occur. Using indirect-access system, the engineer transmits the problem to the programmer who prepares the program. Key-punch operator codes program and scheduler assigns appropriate amount of machine time. Program is executed by machine and results are sent back to engineer. Even minor errors often cause delays. If engineer has not prepared problem correctly, programmer must return it to engineer for clarification. Errors in programming, key-punch operation or scheduling cause the problem to be returned to the programmer. This further increases time to obtain results. Using a small computer, the engineer's direct knowledge of problem aids in problem solution. Errors introduced in machine are immediately apparent and easily rectified by the engineer. The actual computation time is increased, but elimination of transmittal time often decreases the time from problem to answer.*

COMPUTER SOFTWARE

Software is the program used to extend the capabilities of a general-purpose computer. It is with software that the engineer adapts the machine to solve particular problems. The programming techniques are called software to distinguish between machine functions that are built into the machine hardware. In its basic form, the computer offers maximum flexibility when programmed in machine language. Machine language is a basic code that is acceptable to the machine without further modification. To program a computer in machine language requires an intricate knowledge of the computer as well as a thorough knowledge of mathematics. Using only machine language, the computers generally perform addition, subtraction, multiplication and division. Other functions such as trigonometry, roots and powers are generated by using the four basic functions and mathematical techniques. It is through the use of software programs that the engineer communicates with the computer. The software programs convert a language familiar to the operator into the machine language acceptable by the computer. Some programs include subroutines that allow the operator to perform complex mathematical operations with a single command. Other types of programs code instructions, assign machine address locations and combine subroutines. Many software programs are written to solve specific engineering problems.

GLOSSARY

Rather than print an incomplete glossary, EDN refers interested persons to "Automatic Data Processing Glossary". This excellent 62-page booklet is available from the Superintendent of Documents, U.S. Government Printing Office, Washington 25, D. C. The price is $0.40.

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An Introduction to the

RAYTHEON 520 PROGRAMMING LIBRARY

RAYTHEON COMPUTER

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COMPLEMENTING THE RAYTHEON 520 . . .

. . . is the Programming Library, an extensive set of programming aids designed to take full advantage of machine characteristics. The basic elements in the Library are integrated so that they form an extremely effective TOTAL OPERATING SYSTEM. Raytheon makes the entire contents of this Programming Library available to every 520 installation, giving to each user means for exploiting his computing and data processing with minimum programming effort.

The design specifications and the development of the Programming Library are the result of extensive analysis by and with specialists in many fields, each of whom was required to impress his bias on the Library and its contents. Every effort was made to reveal and give consideration to the complete needs of any given 520 SYSTEM configuration in many operating environments. Versatility was also a primary goal in developing the 520 SYSTEM Programming Library. To this end, standard structural characteristics were devised to provide similar frameworks for each of the separate programs. They can thus be considered as modules suitable for combining to form many special-purpose programs simply and quickly. In addition to reducing programming time — which was a primary design specification — this approach simplifies library maintenance activities.

These efforts produced, as the basic component of the 520 TOTAL OPERATING SYSTEM, a highly-sophisticated executive/monitor control routine called BOSS. BOSS provides each user means for continuous and effective operation of his computing installation with a low-cost/high-production yield.

The Programming Library also includes FLEXTRAN®, a newly-conceived, completely flexible translator of the compiler-assembler type; 520 FORTRAN, substantially extended version of FORTRAN II; and an IBM 1620 Simulator. The TOTAL OPERATING SYSTEM also includes a comprehensive set of mathematical subroutines, utility and service routines to allow complete assistance in the operation of the central processor and its many peripheral options, and a completely-automatic, multi-level diagnostic program.

FLEXTRAN® is an advanced syntax-directed programming system of the compiler-assembler type. This type of automatic programming system provides users that extensive linguistic capability that is desirable for ease in developing and testing programs. Thus, a program may be written in a language that is essentially the machine's own natural language or a programmer may create a virtually unlimited set of his own macro-instructions, either for temporary or permanent use. More than 140 such macro-instructions have been defined. The following list is a cross-section sample of these instructions: Table Look Up, Push Down Queue, Floating Compare for Less, Store Address Field of A Register, Double Precision Multiply, Compare A Register and Limits, and Transfer and Set Return. Subsets of them are oriented to particular problem-solving environments. For example, there are instruction sets for the scientific and data systems environments. Thus, FLEXTRAN® and the Raytheon 520 System's natural language combine to provide a programmer with ability to create linguistic capability for every use, including the creation of translators of other computers' source language programs.

Raytheon 520 FORTRAN is a substantially extended FORTRAN II. It includes such features as load and list/link routines, interchange of input/output units without re-programming, the facility to accept any standard FORTRAN II statement, the most extensive diagnostics of any FORTRAN II, and the ability to handle mixed-mode arithmetic. It also has a special feature which allows complete modification (augmenting, diminishing or altering the contents) of the FORTRAN Library to suit the particular needs of a given problem without becoming involved in the complex mechanics of the Library. 520 FORTRAN is especially fast in compiling and generates object programs that require less memory and give faster object execution speeds. It is further enhanced by the very desirable characteristics of being easy to learn and to use.

The 1620 Simulator gives to users of that computer the means to expand their computing capabilities to the level of the faster, high-performance 520 System without the high pressure that often accompanies a changeover, a conversion from one computer to another. Use of the 520 System also provides all the added benefits of the 520 Programming Library. The Raytheon 520 simulates the 1620 to give program execution up to three times faster than the 1620 Mod I.

FORTRAN source programs, incidentally, could be recompiled and executed by the Raytheon 520 at a speed as much as fifty times faster than the 1620.

Finally, Raytheon gives extensive programming support and thorough education and training in computer use. Programming support is provided in the field, at the customer's site, by a staff of competent Computer Applications Specialists assigned to offices from coast to coast. Training includes courses on system operation, programming and maintenance. Membership in the Raytheon Users' Group, which was formed by users for their mutual benefit, is open to users of the Raytheon 520 System. Exchange of program materials and sharing of knowledge about how to exploit effectively their computer systems are primary motives of its members.

Taken together, these programs, routines, languages and services are the basic ingredients of a comprehensive Support Schedule that assures a user he can make efficient and effective use of his 520 System.

BOSS

BOSS, the Raytheon 520 Monitor and I/O Control System, provides automatic control of the operation of the 520 System. BOSS achieves its goal of enabling efficient "hands off" operation of a Raytheon 520 SYSTEM by:

1. Supervising the running of separate jobs; a section of BOSS resides in memory at all times to insure continuous operations and to permit linkage control between and among the programs in the Library.
2. Calling system programs needed to translate symbolic programs from assembler or compiler language to machine language.
3. Supervising loading of programs and library subroutines; providing a "Load and Go" mode, which permits a program to be compiled or assembled and then executed.
4. Supervising the printing of diagnostics and memory dumps as requested by the program or as needed when a program is terminated.
5. Interpreting all basic input/output commands to insure legality and allow them to be executed if they reference a non-restricted and free device.
6. Permitting the accumulation of time for any single job from the time the ID card is interpreted until the end of the job.

THE ASSEMBLER SYSTEM

FLEXTRAN® 520 is an automatic programming system of the compiler-assembler type. It provides the programmer with an extensive capability to ease the writing and testing of programs. This is accomplished in a language that is one-for-one with object code or at a macro level combining many machine instructions in frequently used problem-oriented programming functions.

FLEXTRAN® was designed to provide fast assembly, efficient object code (by means of both generator structure and the directive or declarative forms that allow the programmer to exercise significant control over the compiler-assembler itself), and extensive source-language statements to aid program testing. All of these design points are successfully welded into an automatic programming system that effectively copes with the demand for such a system. With appropriate auxiliary storage, FLEXTRAN® can operate in the "load-and-go" mode.

A FLEXTRAN® program is composed of statements in either imperative or declarative form. An imperative statement is one that is equivalent to one or more of the instructions to be executed by the "target" computer (for example, Add Exponent, Test for Zero). A declarative form (or directive) is one that instructs the compiler-assembler to do something (for example, "BLOC" specifies the beginning location of a program block). A declarative form may also convey information to the compiler-assembler (e.g., "QUIT" marks the end of the program to be assembled). Finally, a declarative form may be ignored by the compiler-assembler (e.g., "*" may be used to identify a statement containing comments only).

In addition to recognizing the 64 instructions that are a 520 System's machine language, FLEXTRAN® permits the use of more than 140 macro instructions. Some of these are oriented to particular kinds of environments. For example, one subset of macro instructions is concerned with data systems applications; it includes instructions like:

Convert Channel N
Test Upper and Lower Limits
Output Word to Control Register
Input 24-bit Data Word from Channel N
Data Quality Check
Convert to Engineering Units

Another set of macro-instructions has been designed specifically to implement the coding of programs for an analog-digital hybrid computer simulation. These include such functions as:

Analog Computer Mode Select
Read Analog Channel and Scale
Scale and Write Analog Channel
Skip on Analog Channel Greater
Skip on Analog Channel Less

Set Pot
Read Pot Setting
Read Analog Element

A specially selected group of the macro instructions are further distinguished as the basic set of general-purpose instructions. So distinguished, they facilitate the sharing of programs written by any user of a Raytheon 520 System.

The programmer has complete control over the format of any segment of the assembled object program. With this control the programmer can make every decision concerning space-time tradeoffs. All necessary housekeeping functions are provided by the compiler-assembler.

The compiler-assembler puts out both absolute and relocatable object code. The loader part of the Raytheon 520 Operating System can load separately assembled programs, irrespective of the sequence in which the segments were assembled; the loader provides all necessary linkage.

All input and output are handled through the Input/Output Control System (IOCS). Input and output are "file oriented;" the concept of a file permits free and easy assignment of peripheral devices. For example, if output to the line printer is file oriented, that output may be reassigned to another peripheral device if the printer cannot be used. Thus, useful work may continue to be done even when part of a system is inoperable.

Each program in the Raytheon 520 Programming Library has a structure that may be listed in either of two groups — Systems or Scientific Applications. Every program — including FLEXTRAN® itself — has the basic characteristics of a subroutine. Thus, the elements of the Library can be regarded as two types of modules, and as determined by the type of problem, may be used as standard building blocks out of which an unlimited variety of special-purpose programs can be constructed with ease and simplicity. Not only is programming effort eased by this artifice, Library maintenance is facilitated too.

RAYTHEON 520 FORTRAN

For the Raytheon 520, FORTRAN II has been extended to give 520 users the most efficient, useful, and convenient programming system available for this class of computers. Some of the outstanding advantages are:

Fast compilation combined with efficient object code

Simplified syntax to save programming time and reduce errors

First-pass source deck error checking and diagnostic printout

Relocatable compiled programs

I/O devices named at object load time to allow interchange without reprogramming

Overlapped computing and block transfer I/O operations

Load-link-list facilities to allow merging of separately compiled programs and simplify debugging

Editor routine to permit easy modification and expansion of FORTRAN Library to fit installation needs

Compatibility with IBM FORTRAN II

These are some of the general features that contribute to making Raytheon 520 FORTRAN the procedure-oriented system with the most benefits for the user. Another set of major advantages results from the elimination of most of the redundancies and logically unnecessary restrictions of earlier versions of FORTRAN. In addition, the meanings of some of the other features have been generalized so that they apply to more situations. These changes have made 520 FORTRAN easier to learn, easier to use without making minor errors, and much more powerful than earlier versions. At the same time, these changes have led to development of a processor capable of both fast compilation and the production of highly efficient object code. The result, from the user's viewpoint, is a welcome saving through strict conservation of time and of memory space during both program generation and actual production.

Raytheon 520 FORTRAN is compatible with 7090 FORTRAN II and compatible with all other FORTRAN II versions given very minor changes. For example, statements may involve components not present in the 520 System. Such a problem can be handled automatically, however, because the Raytheon compiler provides the facility of reassigning input/output devices at object program time.

To illustrate how the restrictions of earlier FORTRAN versions have been overcome for the Raytheon 520, consider the greater freedom in program preparation indicated by these characteristics:

Statement labels may be alphanumeric

Variable names may be up to 40 characters, instead of only six

Standard representation of array elements is allowed in equivalence statements

The replacement operator has been completely generalized

Mixed mode expressions are permitted

Levels of exponentiation are unlimited

Alphanumeric fields may be stored as arrays

A subscript may be any arithmetic expression and may take on negative values

Subscripts may be subscripted

The number of allowable subscripts is unlimited

Assigned GO TO statements have been expanded

In a DO statement, values following the equal sign may be any constant, variable, or arithmetic expression

Reverse DO loops are allowed

A DO loop may be entered from outside its range

Arbitrary rules for writing statements have been removed

Mixed mode input/output statements are allowed

The best way of assessing the advantages of these characteristics, of course, is to compare them to FORTRAN II procedures in actual practice. The following example is a brief illustration of the benefits to be realized. The first set of 17 statements was written under the restrictions imposed by FORTRAN II; it produces 46 instructions for the Raytheon 520. By rewriting these statements to take advantage of the flexibility of Raytheon 520 FORTRAN, we have six statements yielding 29 instructions. Note the twofold saving that results: a 65 per cent reduction in source language and a 37 per cent reduction in object code.

FORTRAN II		RAYTHEON 520 FORTRAN	
	I=ISTAR		
	J=I + 1		
	K=J + 1		K=1 + (J=1 + (I=ISTAR))
110	A=I		
	B=J		
	AB=A * B		
	X=AB/RATIO	110	X=(AB=I*J)/RATIO
115	C=K		
	RP=X/C		
	RPP=RP + .501		
	L=RPP	115	IF((L=(RP=X/K)+.501)−MAX) 400,400,600
	IF (L-MAX) 400, 400, 600		
400	IF (L-K) 600, 401, 401	400	IF(L-K) 600,401,401
401	D=L	401	IF(RP-L) 402,410,403
	IF (RP-D) 402, 410, 403		
403	DP=D + .1	403	IF(L+.1−RP) 600,410,410
	IF (DP-RP) 600, 410, 410		

THE 1620 SIMULATOR

For the convenience of Raytheon 520 users who are making a transition from an IBM 1620, a simulator has been prepared to allow direct execution of the 1620 programs by the 520.

Some general features of the 1620 Simulator are:

All basic and optional 1620 instructions are simulated

Machine-language 1620 programs can be run without reprogramming

Simulated 1620 programs are executed on the 520 as much as three times faster

IBM 1402 Card Reader/Punch units and 1311 Disk Packs from the 1620 System can be used with the 520

Memory requirements for simulation can be seen from the following table:

IBM 1620	RAYTHEON 520
20,000 digits	8,192 words core, 512 BIAX
40,000 digits	16,384 words core, 512 BIAX
60,000 digits	20,480 words core, 512 BIAX

The 1620 Simulator includes provisions for paper tape input and output, typewriter, card reader/punch, and line printers.

The speed advantage of the Raytheon 520 varies according to the type of 1620 program and the field lengths of operands within the program. As an average, a speed ratio of three-to-one in favor of the 520 can be expected. Input/output simulation takes place at the operating rates of Raytheon peripheral devices.

After the Simulator is loaded, a set-up routine produces a request for input describing the equipment

configuration to be simulated. The same routine arranges for the Simulator to operate according to the 1620 specified by the user.

A console routine is provided to give the user control of the simulation process. It supplies a means for the operator to enter data and examine the status of the simulated 1620 console. It also provides indications of error conditions, halts, and peripheral equipment status.

The user is informed of the condition of the simulated console switches and indicators by typewritten messages. Provision has been made for interruption of the automatic operation and inquiries or control by the operator.

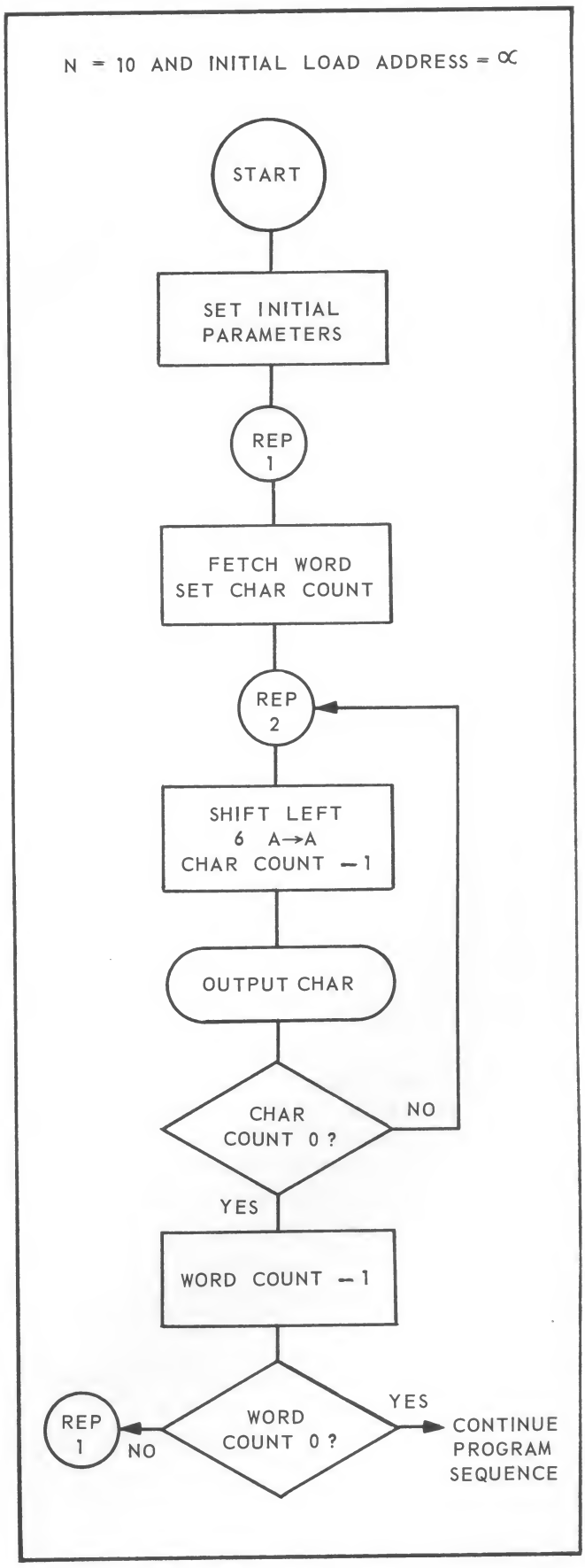
Those programs written in 1620 FORTRAN language can be compiled by the Raytheon 520 FORTRAN processor; the resultant machine code can be executed on the Raytheon 520 without use of the 1620 Simulator at speeds as much as 50 times greater than the speed of the 1620 Mod I.

WRITING IN 520 BASIC LANGUAGE

The Raytheon 520 basic language instruction set provides extensive flexibility for handling of data, especially where individual bits, or fields, of a character, or word, are moved or tested. The instructions are especially well-suited for subroutines where loops are made and for data I/O routines. The routines can easily be made efficient in length and speed. The following is an illustration of the ease with which a data output of N words, each with four 6-bit characters, is made at machine language level (of course, the code is written in basic FLEXTRAN® format):

8-word instruction sequence:

```
        LDI     P,L   set initial load address -> L
                      and loc counter + 1
        LRC     10    set word count -> 10
        ADR     α     initial load address
REP 1   LDI     L,A   load word
        CLD     4     set CHAR count -> 4
REP 2   SLS     A,A   shift left six A -> A
        CDL     D,D   CHAR count - 1
        DTR     2,A   output least significant 6 bits
        NOP
        TNZ     D,F   CHAR count 0?
        BTR     2     no -> REP 2
        CDL     N,N   yes -> word count - 1
        TNZ     N,X   word count 0?
        BTR     5     no -> REP 1
        NOP
        . . .         yes -> continue program
                      sequence
```



Utility Routines . . .

These include routines that provide such assistance as program loads, typewriter I/O, formatted memory dumps, data conversion, card I/O, system editing, magnetic tape I/O, paper tape I/O, paper tape editing, conversion of paper tape to cards and cards to magnetic tape.

Service Routines . . .

Diagnostic routines are provided for both hardware and software. An automatic, monitor-controlled hardware diagnostic with modular construction allows the user to select from the complete set of modules only those that test his hardware. For example, one set of modules can test a minimal system consisting of CPU, Typewriter, Paper Tape Reader and Punch and Line Printer. Modular construction permits easy addition or deletion of test routines as system configurations change, thus enabling the user to achieve economies in storage and maintenance. It provides automatic fault detection with special examination features for each type of failure. The collection of software diagnostics is a comprehensive one. FLEXTRAN® and FORTRAN, of course, are rich in natural linguistic capability to provide dynamic information about program status. In addition, cross-reference listings, for example, aid in developing and testing programs. Also available are selective and complete trace routines, selective dumps, etc.

Mathematical Subroutines . . .

Raytheon provides a comprehensive set of high-speed mathematical subroutines. Routines exist that will accomplish the following tasks:

Polar to Rectangular Coordinate Conversion
Binary to BCD (four 6-bit words)
BCD to Binary (four 6-bit words)
Square Root
Sin
Cos
Arctan
Exponent
Log
Floating Point to Fixed Point
Fixed Point to Floating Point
Angular Unit Measurement Conversion
Fourth Order Euler Integration
Fourth Order Runge-Kutta Integration
Gray to Binary (12-bit)

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RAYTHEON

RAYTHEON COMPUTER

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SP-210

RAYTHEON 520 SYSTEM
PERIPHERAL EQUIPMENT

RAYTHEON COMPUTER

RAYTHEON

RAYTHEON 520 SYSTEM

The Raytheon 520 System provides the most powerful and useful input/output capability available in machines of its class. Input, output, and computing can occur simultaneously. Maximum input-output character rate is four million characters per second; word rate is 1MC.

The Raytheon 520 input/output system consists of the following basic components:

1. The peripheral device controller
2. The peripheral device
3. The bus system of communication
4. The 520 input/output control section

A peripheral device communicates with the 520 through a peripheral device controller. Each peripheral device has its own controller which is connected to the input/output system. This method lends itself to economy in that the user need only order what he must have for his particular 520 system configuration. This also provides ease of system expansion and replacement when more advanced peripherals are available.

The peripheral device controller will respond to computer control commands, will accept and provide synchronizing signals required by the 520 System and the device, will provide word or character buffering with error detection, and will provide any voltage level and impedance matching required. The peripheral device controller frees the computer from constantly checking an input/output operation and indicates to the 520 when any transfer of data should take place.

The input/output bus system consists of three cables connected serially to every peripheral device controller in a 520 System configuration. The input bus can transmit 25 bits of data or status information to the 520 from any peripheral device controller. The output bus has 25 bits of data transmission capability and can transmit either data or peripheral device select information from the 520 to any peripheral device controller. The control bus will transmit the control signals generated in the communications between the 520 and any peripheral device controller. Communication over the bus system is accomplished with current mode signal transmission, providing greater noise rejection and faster signal switching.

Ease of programming has been attained by the use of only two input or output commands and a four-state commutator. The two commands are SELECT and DATA TRANSFER. The SELECT command will put the desired peripheral device controller on-line with the 520. A peripheral device controller must be on-line before anything other than a status response can be accomplished. The DATA TRANSFER command will result in the transfer of data to or from the 520, will send a status response to the 520 from the selected peripheral device controller, or will cause the selected peripheral device controller to go off-line. The commutator is a two-bit binary counter which steps at the clock rate or can be locked to a particular state. The commutator is used to synchronize the transmission of data over the input/output bus by many peripheral devices.

KEYBOARD/DISPLAY STATION 519766

The Keyboard/Display Station is a valuable tool for on line program debugging. Programs are displayed on the Keyboard/Display Station with mnemonic and location in a format identical to the programmer's coding sheet, a "page" of coding at a time.

The editing features of the Keyboard/Display Station are used to make corrections to the program. The programmer may "thumb through the pages" of his program stored in memory just as he can thumb through his coding sheets.

In a data acquisition system, the Keyboard/Display Station may also be used for "quick-look" display of test data or results, as the test progresses. The ability to address locations on the Keyboard/Display Station screen by the computer permits the output of only the changing information by the computer at a 25 μsec. per character rate rather than requiring a complete "page" of information for each change which would require 15 milliseconds.

This light demand on computer time permits a continuous presentation of important test parameters as they change.

SPECIFICATIONS:

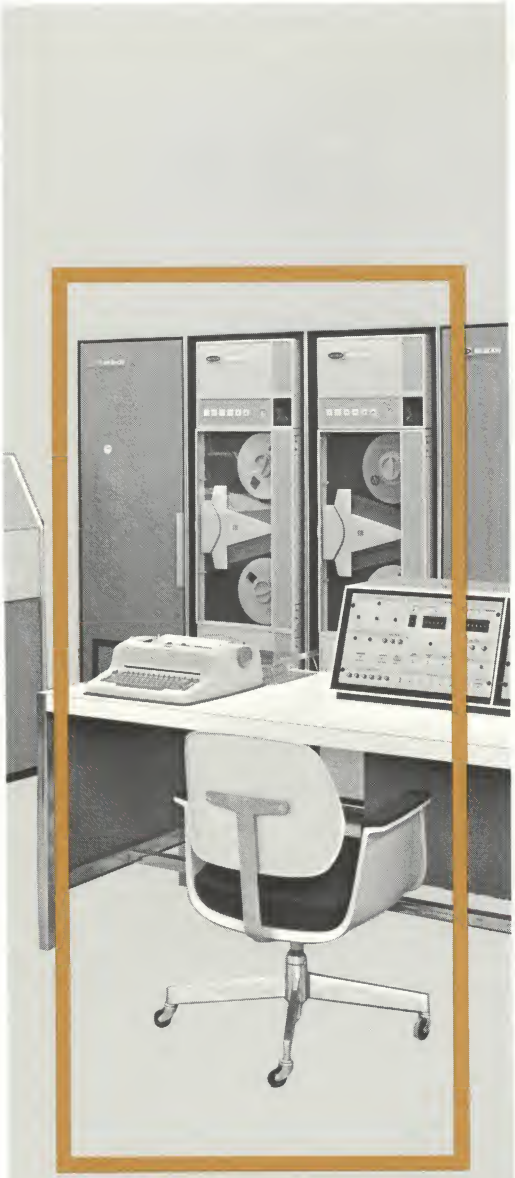
Standard Format: .....13 lines, 40 characters/line
Standard Programming
Character Repertoire: .....64 characters
(Special Character Sets Available at Extra Cost)
Typical Character Size: . . . 0.17 inches high and 0.14 inches wide (can be modified to meet customer requirements).
Display Area on Cathode Ray Tube: .....6½" by 8½"

LINE PRINTER 517857

The Line Printer is an electro-mechanical device for printing data at a high rate of speed. This device is a solid state, self-contained unit which has a full line width buffer, power electronics, and control logic for on-line operation. Operation is fully automatic during programmed printing; however, operator controls are provided for adjusting and positioning paper tension and print. The line printer is designed for edge perforated fanfold paper in multiple carbons or pressure paper. The controller for the line printer is part of the basic I/O chassis in the main frame of the 520.

SPECIFICATIONS:

Printing Speed.....300, 600, or 1250 lines per minute
Line Width.....80, 120, 132, or 160 columns
Characters per column 64
Line Format
Horizontal .....10 columns per inch
Vertical .....6 lines per inch
Printer Size.....56" long x 30¼" wide x 57" high
Power Requirements.....115 VAC, 60 cycle, single phase or 208VAC, 60 cycle, 3 phase, 4 wire or 230VAC, 60 cycle, single phase, 3 wire



MAGNETIC TAPE CONTROLLER 517615

The Magnetic Tape Controller consists of a cabinet with the magnetic tape controller logic chassis, power supplies, and a power sequencer. The controller will respond to all commands from the 520 (SELECT, DATA TRANSFER, DISCONNECT, etc.) and can control up to four transports. The controller will generate and respond to control signals necessary to transport operation (motion control, load point, read clock, etc.). The word format (1, 2, 3, or 4 characters per word) is determined during the selection of the controller. There are two 24-bit registers in the controller. The 24-bit input register can accept a word transfer from the 520 or can assemble a word during a tape read operation. The 24-bit output register can transmit a word to the 520 or can disassemble a word into 6-bit characters during a tape write operation. The controller will generate parity (odd-binary, even-alphanumeric) during a tape write operation and will check the parity during a tape read operation. The controller has control logic for connection of up to four tape transports of the same type (45 ips or 75 ips).

SPECIFICATIONS:

Cabinet size .....75.5" high x 23" wide x 30" depth
Weight .....525 pounds
Power Requirement ....208VAC, 60 cycle, single phase, 4 wire

SINGLE TAPE TRANSPORT/517567

The single Tape Transport has all the design features of the Master Tape Transport except for the data electronics switcher and the control and status line switcher. This unit cannot be used to control tape transports.

MASTER TAPE TRANSPORT 516635

The Master Tape Transport is a medium speed-75 ips-solid state digital tape unit. The Transport features electromechanical tape handling, magnetic head, operator control panel, load point and end of tape sensing and control, file protection, fast and slow rewind, write-read data electronics, data electronics switcher, control and status switcher, and all necessary power supplies. The Master Unit has one set of write-read electronics which can be utilized by the master and up to three slave tape transports. The data electronics switcher directs the data electronics to the proper write-read head in response to a command from the Magnetic Tape Controller (517615). The various controls and status commands are directed to the proper unit by the control and status line switcher. This arrangement allows input/output access to four tape transports through a single input/output channel. The tape transport assembly design features vacuum column tape buffers, counter rotating capstans, solenoid type actuators, positive alignment pinch rollers, and rugged disk-type reel brakes.

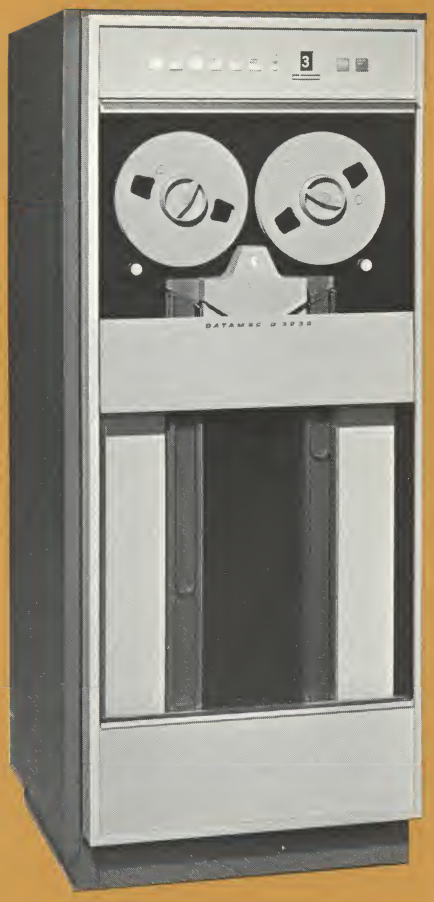
SLAVE TAPE TRANSPORT/516637

The Slave Tape Transport has all the design features of the Master Tape Transport except for write-read electronics, data electronics switcher, and the control and status line switcher.

SPECIFICATIONS:

Tape Speed .....75 ips—forward and reverse
Reels .....10½" diameter, ½" width, (IBM compatible)
Start Time .....5 ms, bi-directional
Stop Time .....1.5 ms, bi-directional
Rewind .....Less than 3 minutes
Tape Density .....200, 556, 800 bpi
Transfer Rates ...15.0 KC at 200 bpi
41.7 KC at 556 bpi
60.0 KC at 800 bpi
Transport size ...69" rack x 30" x 24"
Weight .....390 pounds (516635)
340 pounds (516637)
370 pounds (517567)
Power Requirements .....105 to 125 VAC, 58-62 cycle, single phase

MASTER TAPE TRANSPORT 517628



SINGLE TAPE TRANSPORT/517626

The single Tape Transport has all the design features of the Master Tape Transport except for the data electronics switcher and the control and status line switcher. This unit cannot be used to control slave tape transports.

The Master Tape Transport is a solid state device with the following component assemblies: tape transport, write-read head assembly, photosense, file protect, operator control panel, write-read data electronics, data electronics switcher control and status switcher and all necessary power supplies. The Master Unit has one set of write-read electronics which can be utilized by the master and up to three slave tape transports. The data electronics switcher directs the data electronics to the proper write-read head in response to a command from the Magnetic Tape Controller (517615). The various controls and status commands are directed to the proper unit by the control and status line switcher. This arrangement allows input/output access to four tape transports through a single input/output channel. The tape transport assembly design features vacuum column tape buffer storage, vacuum tape dust and oxide cleaners integral in the head assemblies, short unsupported tape spans to minimize skew and speed variations, and synchronously driven counter rotating capstans with ample reserve power.

SLAVE TAPE TRANSPORT/517630

The Slave Tape Transport has all the design features of the Master Tape Transport except for write-read electronics, data electronics switcher, and the control and status line switcher.

SPECIFICATIONS:

Tape Speed	45 ips—forward and reverse
Reels	10½" diameter, ½" width (IBM compatible)
Start Time	5 ms, bi-directional
Stop Time	1.5 ms, bi-directional
Rewind	3 to 4 minutes for 2400 feet
Tape Density	200, 556, and 800 bpi
Transfer Rates	9.0 KC at 200 bpi 25.0 KC at 556 bpi 36.0 KC at 800 bpi
Transport Size	75.5" high x 23" wide x 30" depth
Weight	425 pounds (517628) 355 pounds (517630) 390 pounds (517626)
Power Requirements	105 to 125 VAC, 58-62 cycle, single phase

DIRECT MEMORY ACCESS

EXTERNAL ACCESS TO MEMORY (EAM)/519731

The External Access to Memory switches memory between the 520 and an external device so the two devices can access memory without interference on a time-shared basis. The external device has priority and can maintain control of memory. EAM interface is standard 520 current mode for both computer and external device.

DIRECT MEMORY ACCESS I/O CONTROLLER/519730

The DMA I/O Controller allows up to four peripheral devices access to memory through the EAM. The DMA I/O Controller is connected to the 520 I/O bus and controls memory through the EAM by presenting the same interface as the computer; i.e., memory address, data out and data in busses, and read and write control signals. It also controls the peripheral devices connected to it through their controllers by presenting the same interface as the 520; i.e.. I/O control, data out and data in busses.

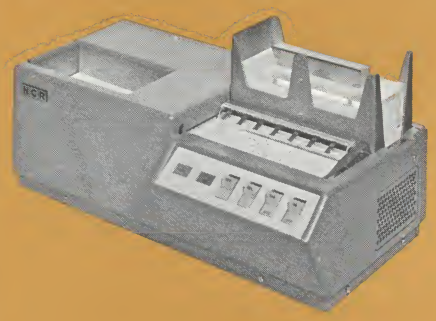
DMA I/O CONTROLLER HIGH SPEED OPTION/519729

Where several devices must be operated simultaneously and one unit must have access immediately, an optional register set eliminates the memory access for control purposes. Each set defines one block of memory with necessary control information.

SPECIFICATIONS:

Maximum Transfer Rate	1 μsec
Connect Time per Channel	2 μsec
Disconnect Time per Channel	2 μsec
Servicing Alternate Channels	200 KC
Number of Channels per DMA I/O (same as 520 I/O)	4
Number of Memory Blocks per Channel	2
Block Lengths	Variable
Block Locations	Variable
Changing Assigned Blocks of a Channel (not computer time)	4 μsec
Word Size	24 bits

CARD READER 517980



The Card Reader is a device which will read standard 80-column punched cards by column at a rate of 100 cards per minute. Under program control a card can be read in the binary mode (12 bits) or can be read in the alphanumeric mode (6 bits). The alphanumeric mode has a Hollerith-to-520 code conversion (12 bits to 6 bits). The card reader is a compact, lightweight unit with convenient access to all controls. Reliable starwheel operated switches are used for data hole detection. The controller for the Card Reader is part of the basic I/O chassis in the main frame of the 520.

SPECIFICATIONS:

Read Speed ....100 cards per minute
Hopper Capacity .....500 cards
Reader Size .....18" long x 10" wide x 9" high
Reader Weight .....25 pounds
Power Requirements .....115VAC, 60 cycle, single phase

CARD READER 519468-001

The Card Reader is a device which will read standard 80-column punched cards by column at a rate of 400 cards per minute. Under program control a card can be read in the binary mode (12 bits) or alphanumeric mode (6 bits). The alphanumeric mode has a Hollerith-to-520 code conversions (12 bits to 6 bits). Both the card reading and the card timing are photoelectric. Simplicity of design results in ease of operation. Cards may be loaded and unloaded during card read operation and extensive error checking results in ease of maintenance. The controller for the Card Reader is part of the basis I/O chassis in the main frame of the 520.

SPECIFICATIONS:

Read Speed ....400 cards per minute
Hopper Capacity .....1,400 cards
Stacker Capacity .....1,000 cards
Reader Size .....18" high x 22" wide x 30" depth
Reader Weight .....125 pounds
Power Requirements .....115VAC, 60 cycle, single phase

CARD READER 519468-002

The Card Reader is a device which will read standard 80-column punched cards by column at a rate of 800 cards per minute. Under program control reading may be binary (12 bits) or alphanumeric (6 bits). The alphanumeric mode has a Hollerith-to-520 code conversion (12 bits to 6 bits). Solid state electronics are used for photoelectric hole detection, card timing pulses, and error checking circuitry. Error checking includes throat jam check, transport check, output hopper jam check, photo diode check, and timing photo diode check. All controls have easy access; card handling during operation is facilitated by simplicity of console design. The controller for the Card Reader is part of the basic I/O chassis in the main frame of the 520.

SPECIFICATIONS:

Read Speed .....800 cards per minute
Hopper Capacity .....2,500 cards
Stacker Capacity .....2,000 cards
Reader Size .....40" high x 29" wide x 33" depth
Reader Weight .....325 pounds
Power Requirements .....115VAC, 60 cycle, single phase

CARD READ-PUNCH 503948

The Card Read-Punch is a device which can read standard 80-column cards at 800 cards per minute and punch cards at 250 per minute. Card reading and punching are by row with independent reading and punching achieved through the use of an opposing feed design. The Card Read-Punch unit has easy access to all operating mechanisms and the operator control panel. Ease of card handling in both hopper and stacker, sensitive misfeed detection, and automatic shutdown for prescribed events (full stacker, transport jam, etc.) are incorporated in both read and punch feed mechanisms.

SPECIFICATIONS:

Read Speed .....800 cards per minute
Punch Speed .....250 cards per minute
Hopper Capacity Reader .....3000 cards
Punch .....1200 cards
Stacker Capacity Reader .....1000 cards
Punch .....1000 cards
Unit Size.....62" high x 58" wide x 30" depth
Power Requirements....208 VAC, 60 cycle, 3 phase, 4 wire

CARD READ-PUNCH CONTROLLER 517614

The Card Read-Punch Controller consists of a cabinet with the card controller logic chassis, power supplies, a power sequencer, and a remote power supply for the Card Read-Punch unit. The controller synchronizes all data and control signals between the Raytheon 520 and the Card Read-Punch. The controller has an 80-bit buffer for the Card Punch and an 80-bit strobe circuit for the Card Reader. Simultaneous reading and punching, error condition checking, data analysis, format control, and Card Read-Punch operations are under the control of the 520 through the Card Read-Punch Controller.

SPECIFICATIONS:

Cabinet Size .....75.5" high x 23" width x 30" depth
Weight .....:.500 pounds
Power Requirements ..208 VAC, 60 cycle, 3-phase, 4 wire

CARD PUNCH CONTROLLER/518686

The Card Punch Controller consists of a cabinet with the card punch controller logic chassis, power supplies, and a power sequencer. The controller will respond to all commands from the 520 (SELECT, DATA TRANSFER, DISCONNECT, etc.) and can control one card punch unit. The controller will generate and respond to control signals necessary to card punch operation (card feed, reset punch buffer, etc.). The controller contains an 80-bit punch buffer for row mode operation with all data formatting controlled by the 520.

SPECIFICATIONS:

Cabinet Size .....75.5" high x 23" width x 30" depth
Weight .....500 pounds
Power Requirements ..208 VAC, 60 cycle, 3 phase, 4 wire

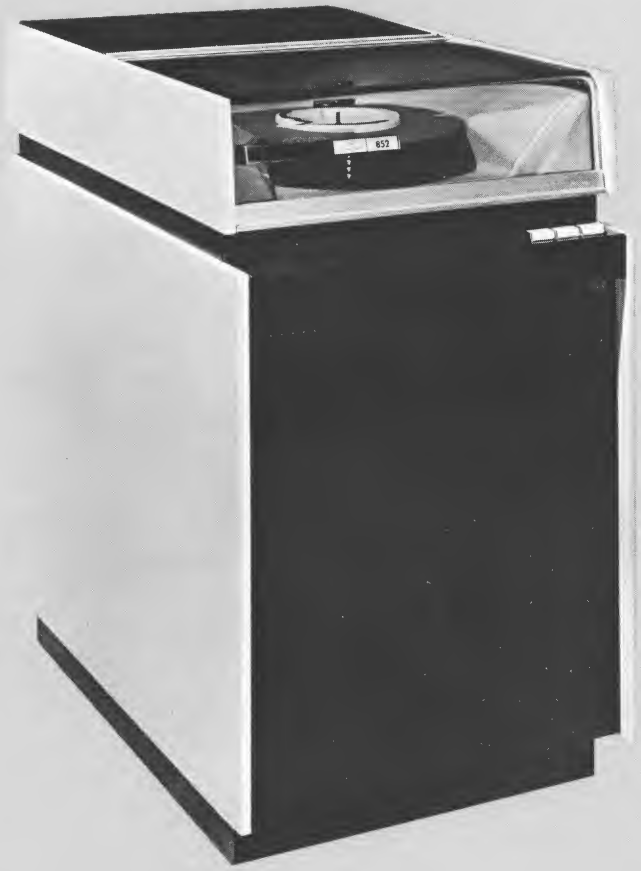
CARD PUNCH/519467

The Card Punch is a device which will punch standard 80-column cards at the rate of 100 cards per minute. The cards are punched by row under control of the Card Punch Controller.

SPECIFICATIONS:

Punch Speed .....100 cards per minute
Hopper Capacity .....800 cards
Stacker Capacity .....1,000 cards
Unit Size .....50" high x 50" width x 25½" depth
Power Requirements .....115 VAC, 60 cycle, single phase

DISK PACK UNIT 517971



The Disk Pack Unit is a device which provides a fast, efficient means of information storage and retrieval. Information is stored on removable disk packs which can be interchanged between units without restriction. A disk pack can store 2 million alphanumeric characters when written in the sector mode or 2.98 million when written in the track-record mode. The access mechanism has ten read/write heads which track horizontally across the disk pack surface during a seek operation. Direct seek is a standard feature which reduces access time when changing tracks. Each of the ten surfaces has 100 tracks which can be divided into sectors (20 per track) or records (1 per track). The cylinder concept is used in the addressing of the access mechanism for IBM compatibility.

SPECIFICATIONS:

Physical Size .....40¾" high x 36" long x 24" wide
Weight .....480 pounds
Storage Capacity .....sector mode: 2,000,000 characters
track-record mode: 2,980,000 characters
Tracks per Surface 100
Read/Write Heads 10
Maximum Access Time .....145 ms.
Maximum Latency Time ...40 ms. (1500 rpm disk speed)
Track to Track Access Time .....30 ms.
Character Definition .....7-bit BCD
Addressing .....IBM Compatible
Recording Method .....NRZI
Average Data Transfer Rate.sector mode: 50,000 char/sec.
track record mode: 74,500 char/sec.
Power Requirements .....208 VAC, 60 cycle, three phase

DISK PACK CONTROLLER 517970

The Disk Pack Controller consists of a cabinet with the disk pack controller logic chassis, power supplies, and a power sequencer. The controller will respond to all commands from the 520 (SELECT, DATA TRANSFER, DISCONNECT, etc.) and can control up to four disk pack units. The controller will generate and respond to control signals necessary to disk pack operations (read/write control, head select, track select, etc.). The addressing format follows the cylinder concept with either sector mode or track-record mode. A cylinder can be defined as a vertical plane which contains ten tracks. Since the disk pack unit has ten read/write heads located in the same relative position on each surface there is no movement of the access mechanism when operating within a cylinder. Sequential operation within a cylinder can access up to 200 sectors with one command. Two 24-bit registers provide word buffering during read/write operations with automatic parity generation and checking.

SPECIFICATIONS:

Cabinet Size .....75.5" high x 23" width x 30" depth
Weight .....600 pounds
Power Requirements ..208 VAC, 60 cycle, 3 phase, 4 wire

DISK PACK/517972

The Disk Pack is a precision device which has six disks mounted ½" apart on a vertical shaft. Each disk is 14" in diameter and has two surfaces coated with magnetic iron oxide for recording information. Each surface has one hundred data tracks which are .020" apart. The inner track is 9" in diameter and the outer track is 13" in diameter. The six disks provide ten surfaces for recording data as the upper surface of the top disk and the lower surface of the bottom disk are not available due to protective plates. Each disk pack is removable and interchangeable between units. Each disk pack can store 2 million alphanumeric characters when written in the sector mode or 2.98 million characters when written in the track-record mode.

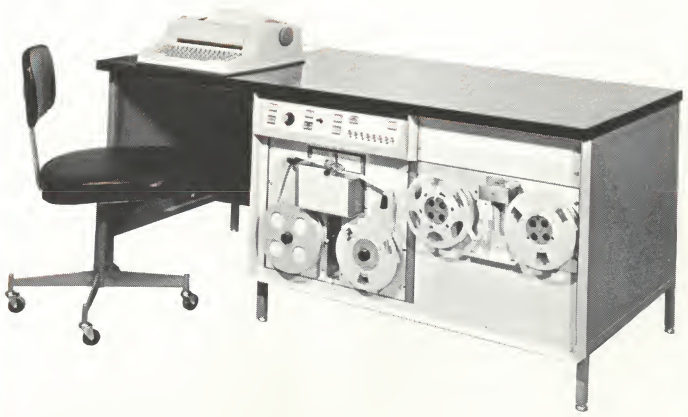
TYPEWRITER 517856/517733

The Typewriter is a 64-character input/output device capable of typing at rates up to 15 characters per second. Characters typed out by the typewriter are spaced 10 to an inch horizontally and 6 to an inch vertically. Unique design features include high print speed and a stationary carriage. The Typewriter accepts coded parallel bits (7 bits, including check) for alphanumeric printout. In addition, it generates coded parallel bits from keyboard operation for input purposes. Remote shift, line feed, backspace, solenoid operated keyboard lock, and end of line indication are provided as standard equipment. The controller for the Typewriter is part of the basic I/O chassis in the main frame of the 520.

SPECIFICATIONS:

Printing Cycle	15.5 cps.
Cycle Time	65.5 ms.
Carrier Return and Tabulation	17" per second
Shift Cam and Clutch	15.5 cps.
Backspace	15.5 cps.
Spacing	15.5 cps.
Type Element	913 (programming)
Writing Line Length	13" Rack Mounted (517856)
	13" For Console Mounting (517733)

TAPE PREPARATION UNIT 516850

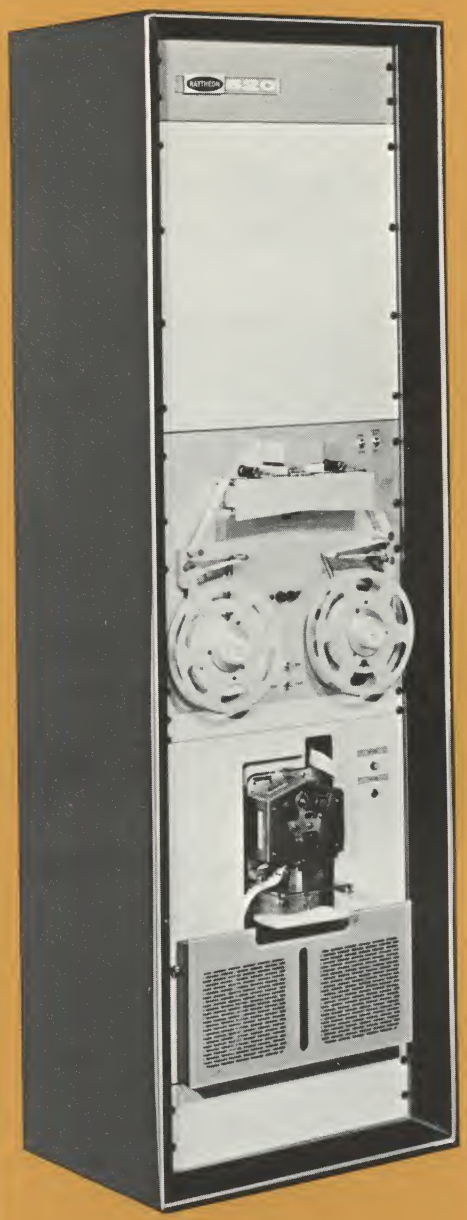


The Tape Preparation Unit is an off-line preparation desk equipped with a typewriter, a paper-tape punch with supply and take-up reels, and a paper-tape reader with bi-directional tape reading capability.

Five operating modes are available on this unit: read-type-punch, read-punch, read-type, type-punch, and type. Other features: 7-bit (alphanumeric) 8-bit (binary) code select, single character read (forward or reverse), parity error and reader error indicators, and 8-bit stop code selection which provides for any 8-bit code to be punched or searched for on the reader.

SPECIFICATIONS:

Height	29 inches
Width	30 inches
Length	67 inches
Weight (including electronics)	375 pounds
Reader Speed	60 cps.
Punch Speed	20 cps.
Typewriter Speed	15.5 cps.



PAPER-TAPE READER/517622

The Paper-Tape reader is a photo-electric reader that will read up to eight-channel punched paper tape at a rate of 300 characters per second in either the forward or reverse direction. The paper tape may be read in either binary (8-bit) or alphanumeric (7-bit plus parity bit) mode. The controller for the paper-tape reader is part of the basic I/O chassis in the main frame of the 520.

SPECIFICATIONS:

Speed	300 characters per second
Direction	Bi-directional
Tape	Tape Guide Adjustable for 11/16" or 1" Tape
Start Time	8 ms.
Stop Time	0.5 ms.

PAPER-TAPE SPOOLER/530507

The Paper-Tape Spooler is a bi-directional device which can automatically supply tape *to* and take up tape *from* the paper-tape reader at the proper speed and tension. Rewind operations can be performed in either the forward or the reverse direction.

SPECIFICATIONS:

Tape Speed, Servo Mode	0-30 inches per second
Tape Direction, Servo Mode	Bi-directional
Rewind Speed	200 inches per second, bi-directional
Tape Width	tape reel for 11/16" and 1" tape

PAPER-TAPE PUNCH/517624

The Paper-Tape Punch is a high speed electro-mechanical device which records information under program control on paper tape at speeds up to 110 characters per second. A high carbon steel punch pin assures positive tape perforation and long pin life. A self-adjusting brake mechanism provides positive control for rapid starting and stopping movements of the tape reel. An all steel cover and resilient rubber motor mounts reduce noise and absorb vibration. Information will be punched in either binary (8-bit) or alphanumeric (7-bit plus parity) mode. The controller for the paper-tape punch is part of the basic I/O chassis in the main frame of the 520.

SPECIFICATIONS:

Speed	110 characters per second
Capacity	1,000-foot roll of tape
Characters per inch	10 characters
Tape Dimensions	11/16" tape with 5 level code 1" tape with a 6, 7, or 8 level code

DRUM MEMORY

For applications where fast access and transfer rate to bulk storage are needed, the 520 System utilizes a high-speed, random access Drum Memory system. Maximum access time to the Drum is 10 milliseconds and transfer rate to and from the Drum is 50,000 words (200,000 characters) per second. Maximum data storage on the Drum is 262,144 words (1,050,624 characters). The Drum input/output controller will accommodate up to four Drum Memory units.

MAGNETIC DRUM MEMORY/519808

The Magnetic Drum Memory is a device which offers large memory capacity with fast access time. The recording surface has 256 data tracks and each data track has 512 words. The Magnetic Drum has eight timing tracks which are used by the controller to synchronize data transmission. A separate read/write head is provided for each track which allows simplicity of design and eliminates time consuming search and positioning operations. The unit is compact and is shock-mounted on a standard 19-inch slide rack.

SPECIFICATIONS:

Speed	6000 RPM
Access Time	5 milliseconds, average
Word Density	512 words per track
Tracks	256
Total Words per Unit	131,072
Word Time	19.5 microseconds
Physical Size	19" diameter x 18" high
Weight	100 pounds
Power Requirements	115/208 VAC, 400 cycle, 3 phase, 4 wire

MULTIDEVICE CONTROLLER/517975

To meet the need of the computer data systems market, Raytheon Computer has designed a simplified and generalized computer interface, the Multidevice Controller, which is intended to be equivalent to a "Real-Time Data and Control System Package." The design philosophy employed recognizes the fact that customer capability has increased in recent years to the point where extensions of a basic logical design may be implemented with standard digital modules by virtually all laboratories making use of data systems equipment.

The Multidevice Controller (MDC) utilizes standard Raytheon Computer modules, power supplies, and mounting hardware. The MDC may be supplied in a low cost minimum configuration which may be expanded as required in the field by plugging in additional digital modules and/or by installing standard pre-wired sub-assemblies. It is practical to implement almost any imaginable system requirement in this manner. The standardized hardware and techniques result in lower cost, simpler and easier to maintain systems. In addition, modifications require far less time and effort.

MDC OPTION—MULTIDEVICE CONTROLLER EXPANSION/517976

This is an expansion of the device addressing capability of the MDC in increments of eight. The device addressing capability can be expanded in increments of eight to 512 devices.

MDC OPTION—REAL TIME CLOCK/517979

The Real Time Clock is a 24-bit system with a one megacycle or external clock input. This system can be read out or set to a desired configuration by command of the 520. The system can be connected to the normal or priority interrupt system for overflow detection.

MDC OPTION—FOUR-LEVEL PRIORITY INTERRUPT/517977

One of the optional features available with the MDC is a priority interrupt system which begins with four levels of priority and is expandable in increments of four to 32 levels. This permits a hardware priority level assignment which can be changed, at the requirement of the user, by changing the wiring to a patchboard.

The system examines all levels for the presence of an interrupt. When at least one interrupt is present, the system determines which has priority. Unless an interrupt of higher priority is being processed, the system will send an interrupt to the 520 and will generate an address unique to the priority interrupt. The 520 will acknowledge the interrupt and transfer to the subroutine to process the priority interrupt. The priority interrupt will be processed, unless interrupted by a higher priority, and will indicate completion to the priority interrupt system.

MDC OPTION—PRIORITY INTERRUPT SYSTEM EXPANSION/517978

This is an expansion of the Four-Level Priority Interrupt system by four levels. The four-level priority interrupt system can be expanded in increments of four to 32 levels.

Another option permits expansion of the priority interrupt system to 1024 levels in increments of two.

MDC OPTION—ASSEMBLY REGISTER/519469

The 24-bit Assembly Register can assemble one 24-bit word, two 12-bit words, three 8-bit words, or four 6-bit words. The determination of word size to be assembled can be program controlled or fixed externally by pin assignment. When the register is fully loaded, an interrupt will be generated.

POWER FAILURE PROTECTION SYSTEM/519470

The Power Failure Protection System monitors the AC input line to the 520. In the event of power failure, normal program sequence is interrupted and program control is transferred to a register save program. The register save program executes from a diode matrix memory and stores all the addressable registers and toggles into core memory. The location in core memory for register and toggle storage can be specified by the user when the system is purchased. Computer operation is halted at the termination of the register save program.

MAGNETIC DRUM CONTROLLER 519809

The Magnetic Drum Controller consists of a cabinet with the magnetic drum controller logic chassis, power supplies, power sequencing and the mounting for one magnetic drum unit. The controller will respond to all commands from the 520 (select, data transfer, disconnect, etc.) and can control up to four magnetic drum units. The controller will generate and respond to control signals necessary to magnetic drum operation (read/write control, ready line, etc.). The addressing format is word oriented and can be either random or sequential. Direct addressing to 1,048,576 words with automatic parity generation and checking is standard. Two 25-bit registers provide word buffering during read and write operations. In a sequential mode of operation track switching and disk switching is automatic with addressing required at the beginning of the operation only.

SPECIFICATIONS :

Cabinet Size	75.5" high x 23" width x 30" depth
Weight	650 pounds
Power Requirements	208 VAC, 60 cycle, 3 phase, 4 wire

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RAYTHEON

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SP-200B

RAYTHEON 520 SYSTEM

RAYTHEON COMPUTER

RAYTHEON

RAYTHEON 520 SYSTEM

the new price-performance leader in scientific, engineering and data systems computing.

The Raytheon 520 System is an integrated, highly automated combination of modern high-speed hardware and state-of-the-art software. It is modular, and Raytheon Computer can design a system to fit your need and budget by selecting the appropriate standard units.

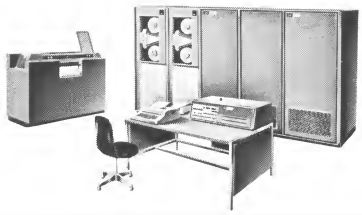
Raytheon has recognized that the day of the "stand-alone" computer is passing, and that customers must have a processor which can be the central element of an expandable automatic data collection and computing system. Sophisticated, high-speed internal operation, and expandable, high-throughput input-output are both essential to good system performance. A wide range of peripherals providing for use of all input-output media and for disk pack mass storage, as well as magnetic tape, are available as system building blocks.

Unusual skill in realtime system engineering is a Raytheon plus. Broad experience and capability in communications, radar, sonar, laser, and photographic data transmission and processing is brought to bear on commercial systems.

Data system implementation and cost are reduced by hardware oriented toward interface of the 520 System with analog computers, satellite telemetry, automatic test and checkout, teletypewriter networks and other data sources.

Software is the key to 520 System superiority. Programming ease and economy, use of an existing program library, speed of processing, and automation of system operation are all planned for your benefit. You may use advanced 520 FORTRAN or FLEXTRAN, Raytheon's advanced compiler-assembler. The use of existing program libraries with the 1620 Simulator or FORTRAN is possible with the Raytheon 520 System. Maximum system productivity and maximum use of programmer or operator labor can be realized when BOSS, the 520 System operating system, is used to control job processing and routine functions.

Raytheon invites you to learn more about its 520 System and to take advantage of the problem solving capability and support that Raytheon Computer will provide.



SUMMARY OF 520 SYSTEM CHARACTERISTICS

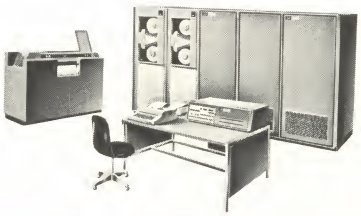
- Fully Parallel Machine Organization
- Twenty-four Data Bits plus One Parity Bit per Word
- 4096 Word Core Memory Modules — Each with Read/Write Electronics
- Two-Microsecond effective Memory Cycle Time
- Direct Addressing to 32,768 Words
- Optional 200 Nanosecond access NDRO BIAX Memory in Modules of 256 or 512 Words
- High-Speed Arithmetic Operation — e.g. One Microsecond ADD and Three Microsecond 10 x 24 MULTIPLY
- 45 One Microsecond Commands
- Two Instructions per Word — Allows Efficient Utilization of Memory
- Seven Addressable Hardware Registers
- Efficient Register-to-Register Instructions — Reduces Time Consuming Memory References
- Most Shifting and Branching Capability in Price Class
- Register Layout Optimized for Floating Point Operations — Allows Intermixed Use of 16, 24 or 39-bit Mantissa Formats
- Sixty-four wired-in Commands, each with many Variations
- Advanced Four-Level Interrupt System included in Basic Processor
- True I/O Bus Structure
- Directly Address up to 512 I/O Devices
- Four 24-bit I/O Channels
- Each I/O Channel may be Time-Multiplexed among many Devices
- I/O Devices Individually Buffered for Simultaneous I/O and Compute
- Wide Range of Peripheral Equipment available
- Direct Memory Access from I/O Devices
- Low-cost Real-Time Data System Interface — Allows Easy System Expansion or Modification
- Advanced Software

  BOSS, the 520 Operating System
  FLEXTRAN Compiler-Assembler
  520 FORTRAN II and IV
  1620 Simulator

520 APPLICATIONS

- Aerial survey data reductions
- Antenna and telescope control (tracking)
- Automatic checkout systems
- Circuit analysis
- Command and control (DOD)
- Communication switching systems
- Component test
- Civil engineering calculation
- Data acquisition systems
- Data reduction
- Digital simulation
- Flight test data processing
- Hybrid computing
- Inventory control
- Lab and process instrumentation
- Launch control and ground guidance
- Map making
- Medical monitoring (hospital)
- Medical research
- Meteorology
- Missile design and analysis
- Mission control
- Nuclear Reaction (monitoring and control)
- Nuclear research
- Oceanography
- Photogrammetry
- Physics (experimental data reduction)
- Radar data reduction
- Reactor design and simulation
- Satellite checkout
- Seismic data reduction
- Statistical analysis
- Structural data reduction (vibration, stress/strain)
- Telemetry (Command and Control)
- Telemetry (flight test, data gathering and reduction)
- Trajectory computations
- Typesetting
- Wind tunnel vibration data analysis reduction

RAYTHEON 520 SYSTEM — THE CENTRAL PROCESSOR



The Raytheon 520 System offers a series of exclusive individual features which provide the user with computing and programming capabilities generally found only in systems costing many times the price of the 520.

The Raytheon 520 System is a parallel digital computer, using a data word of 24-bits plus a parity bit. Forty-five of its 64 basic instructions execute in one microsecond. Effective main memory cycle time is 2 microseconds and a Raytheon-manufactured non-destructive readout memory (BIAX) with an access time of 200 nanoseconds is available as an option.

Basic main memory storage capacity is 4096 words, expandable to 32,768 words. The optional NDRO BIAX memory can be employed in modules of 256 or 512 words.

Use of advanced circuitry, e.g., high speed adder with 5 nanosecond per bit transfer times, allows ultrafast, variable length multiply and divide. Simple multiply executes in 0.5 microsecond plus 0.25 microsecond per bit or eight, twelve and 24 bits in 2.5, 3.5 and 6.5 microseconds, respectively. Full word divide executes in 12.5 microseconds.

SEVEN PROGRAMMABLE REGISTERS

Seven hardware arithmetic registers and an appropriate complement of efficient register-to-register commands are available to the programmer. Since the Raytheon 520 System register-to-register instructions execute in a fraction of the time required for typical computer memory load and store times, the use of multiple registers results in faster throughput rates. For instance, many types of problems require temporary holding of intermediate results. If held in a register, these intermediate answers require no memory access time. Each register may serve as an accumulator or as an index register. As a result, the implementation of exceptionally fast subroutines and highly efficient interpretive and compiler languages may readily be achieved.

RAYTHEON 520 REGISTERS

	Register Name	Use	
Programmable Registers	A	Arithmetic Register	24 bit
	B	Arithmetic Register	
	C	Arithmetic Register	
	D	Arithmetic Register and Command Interpretation Register	
	L	Command Location Counter, General Address Register or Index Register	15 bit
	P	Instruction Location Counter	
	N	Repeat Count Register or Exponent Register	8 bit
	Q	Phantom Register (source of zeros or ones)	
	E	Instruction-Pair Register (not addressable)	
Carry Toggles		Indicate carry from bit positions 0, 1, & 9	
Program Flags		6 1-bit registers	
Parity Toggle		Indicates parity of the last memory access operation	

CONVENIENT DATA DISPLAY

The contents of any arithmetic register or core memory cell may be displayed or changed without disturbing the processing unit. An automatic address halt mode causes the computer to stop when a specified memory location is addressed. Marginal checking voltages are supplied on each power supply. These features provide powerful program debugging and maintenance aids. Six addressable program flags (one-bit registers) and six sense switches are provided for convenience.

ADVANCED MULTI-LEVEL INTERRUPT

An advanced four-level interrupt system is included in the basic system, and is based on a free-running scanner (similar to large scale computer systems). The scanner sequentially tests each channel at a four-megacycle rate. When an interrupt signal is found, the scanner is locked on the requesting channel and the program transferred to one of four fixed positions in memory. Three modes of operation are available and under program control:

(1) Automatic interrupt with program assignable priority levels,
(2) Automatic interrupt with all channels having equal priority levels or
(3) Programmed interrupt.

Programmed interrupt is obtained by manipulating a mask register to inhibit the automatic mode on one or more channels. Input levels to the mask register may be directly tested under program control. The scanner is released under program control to restart from any desired channel, e.g., from channel one in the automatic priority interrupt mode. Automatic and programmed interrupt modes may be intermixed.

The basic interrupt system may be expanded in increments of four levels to thirty-two levels of automatic priority interrupt with an optional system which develops a unique 15-bit address for each priority level. In addition, automatic program jumps for I/O faults allow unique direct servicing for each I/O device. The interrupt features allow exceptionally efficient management of a complex system.

SUPERIOR DATA TESTING AND CONTROL CAPABILITY

More data testing and control capability is provided in the Raytheon 520 System than is offered on any other commercially available computer. This capability includes direct testing for zero *or* non-zero on: (1) the sign, exponent, fraction, magnitude, or logical (entire word) fields in any register; (2) bits 0, 1, 6, 7, 8, 9, 10, 11, or 23 in any applicable register; (3) any one of the six program flags; (4) any one of the six sense switches; (5) any one or all three carry toggles at the same time; (6) any one of the four interrupt mask bits; and (7) any one of four interrupt lines when not in the automatic interrupt mode. In addition, bits 6, 7 and 8 may be tested simultaneously for any 3-bit pattern. *Each of the above testing operations requires only one microsecond.*

UNIQUE DATA SHIFTING PROVISIONS

The Raytheon 520 has shifting capabilities which are unique in the industry. Shifting is applicable to all seven arithmetic registers at speeds up to 500 nanoseconds/bit. There are 84 shifting combinations. Any register may be shifted left or right, open or closed or logical or magnitude fields. Other combinations include a normalizing shift for sign, exponent, fraction or any combination of these, and a shift right double length floating mantissa fields. In addition, the 520 can shift left six bits from any register into any other register in one microsecond.

OPTIONAL NON-DESTRUCTIVE READOUT MEMORY

An optional fast memory may be employed in the 520 System. This memory is of the NDRO (Non-Destructive Readout) type, does not require a rewrite cycle after each read cycle, has an access time of less than 200 nanoseconds, and allows any register to be loaded in only one microsecond. Fast memory is particularly useful for storing frequently used subroutines and substantially improves the throughput of the system. For instance, fast memory reduces the average time for a 24-bit mantissa floating add, not including the calling sequence, from 32 to 17 microseconds. This fast memory, known as BIAX for its multi-aperture ferrite storage element, is manufactured by Raytheon Computer.

RAYTHEON 520 SYSTEM PERFORMANCE

FLOATING POINT OPERATIONS

In general, computer floating point operations may be implemented with either software subroutines or special purpose hardware. Because of its speed and optimized register layout, the 520 System can execute programmed floating point operations at speeds competitive with expensive hardware options for other machines. These highspeed operations can be executed in any one of three floating point formats.

Utilizing 8-bit exponents, mantissa lengths of 16, 24, or 39 bits, including sign, are available. The 24-bit times are fastest, since this format requires less manipulation. The unusual 16-bit format is efficient, since exponent and mantissa are packed into one word. A 16-bit mantissa is adequate for many system applications where 12-bit data is typical. Note that the 16-bit and 39-bit formats are identical, except for mantissa length. This allows efficient intermixing of the short and long formats within one program.

THE RAYTHEON 520 SYSTEM OUT-PERFORMS COMPETITIVE MACHINES

Compared to other computers in its price class, the Raytheon 520 System displays a substantial speed advantage in scientific, engineering and data systems applications. Some of the specific operations in which the 520 demonstrates this advantage are detailed in the table on page 7.

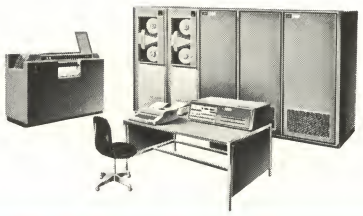
Almost every computer programmer approaches and solves a problem in a different manner. Timing of the operations chosen to illustrate the 520 System's performance superiority are undoubtedly subject to such variations in approach and methods. To minimize the effect of these variables and to ensure overall accuracy, all times for performance of the listed operations on competitive computers were derived from detailed study and application of published programming and reference manuals by professional programmers who, in many cases, were able to draw on actual experience with the machines being compared.

FORTRAN Benchmark tests of 520 System speed will effectively demonstrate overall system superiority.

FLOATING POINT OPERATION TIMES (In Microseconds)*

OPERATION	Subroutine In NDRO Memory			Subroutine In Core Memory		
	16-Bit	Mantissa 24-Bit	39-Bit	16-Bit	Mantissa 24-Bit	39-Bit
ADD**	25-42	21-36	34-45	31-57	29-52	47-64
SUBTRACT**	27-44	23-38	36-47	34-60	32-55	50-67
MULTIPLY	37-39	25-28	74-76	48-51	34-38	95-98
DIVIDE	42-44	48-53	112-129	56-59	65-73	135-157

*Includes subroutine calling sequence of eight microseconds in core memory.
**Assumes an average of two bits of shifting to scale mantissa.



DERIVED TIMES IN MICROSECONDS INCLUDING MEMORY CYCLE

OPERATION	RAYTHEON 520 with NDRO Memory	RAYTHEON 520 w/o NDRO Memory	SDS 930	CDC 3100	IBM 360/40
SCIENTIFIC/ENGINEERING FUNCTIONS					
Floating Point Add (24-Bit Mantissa)	21-36*	29-52	81	NA	43**
Floating Point Add (39-Bit Mantissa)	34-45*	47-64	NA	210†	NA
Floating Point Multiply (24-Bit Mantissa)	25-28*	34-38	59	NA	105**
Floating Point Multiply (39-Bit Mantissa)	74-76*	95-98	NA	340†	NA
REAL-TIME DATA SYSTEMS FUNCTIONS					
Add Register-to-Register	1	1	NA	1.8	7.5
Convert to Eng. Units (12-Bit Data) (ax + b)	10.5	15.5	19.25	21.5	81.26
Normalization $\left(\frac{x-z}{f}\right) \rightarrow y$	14.5	20.5	31.5	22	216.26
Convert any 6-Bit Code to any other code	1	2	8.75	5.25	17.5+6.25/CH.
Binary to BCD Conversion (4 Six-Bit Char.)	24.5	32.5	112	77.5	<50
BCD to Binary Conversion	18	28	80.5	72	<45
Data Quality Check (Match 24-Bit Word Against Reference Word and Count Unmatched Bits)	16	23	69	49.4	108
Limit Check Two 12-Bit Data Words for Upper and Lower Limits	12	20	28	15.2	100.5

*Times for subroutines in fast memory and calling sequence in main memory.
**Short format (24-Bit Mantissa and 7-Bit hexadecimal exponent) with floating point option.
†36-Bit Mantissa

SOFTWARE

- BOSS, the 520 Operating System
- FLEXTRAN Compiler-Assembler
- 520 FORTRAN II and IV
- 1620 Simulator

These 520 System software packages are designed to ease the programmers' efforts in writing and debugging, and to maximize management's return on investment by automating the processing of jobs and utilizing existing program libraries. The following software packages are among those available:

BOSS, THE 520 OPERATING SYSTEM

Raytheon brings to the 520 System user automated operation and productivity previously reserved for scientific computers of larger classes. The 520 Operating System provides several important benefits — automatic assignment and control of input-output, control and batch processing of jobs, time accounting and other housekeeping operations. The 520 Operating System is used when on-line debugging is not taking place, and when high production per dollar invested is desired by the operating management. It supplies control of those processors and routines which provide the capabilities of compilation, assembly, loading, program execution and continuous system operation. Inter-mixing of job types and the compile/ execute and assembly/execute modes are provided. Scheduling jobs is the responsibility of facility personnel.

Dynamic core dumps during program execution and post mortem dumping are accomplished under control of BOSS.

An editor routine provides the capability of modifying, adding, deleting, or replacing system routines and programs stored in the library.

FLEXTRAN COMPILER-ASSEMBLER

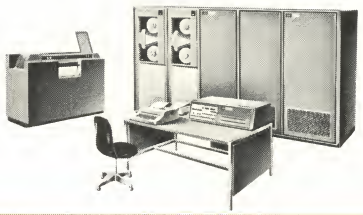
FLEXTRAN is an automatic programming system of the compiler-assembler type. It provides the programmer with many capabilities to ease the writing and testing of programs. In addition to mnemonics for each machine instruction, a standard set of macro instructions is incorporated.

FLEXTRAN allows the addition of new macro instructions either temporarily or permanently as the user requires. Thus macro instructions oriented toward particular applications are possible; for example, one may create macros that facilitate the translation of programs for other computers to 520 machine language.

FLEXTRAN is capable of producing efficient object programs suitable for computer based data systems where realtime throughput must be maximized. It was created with applications such as data acquisition, telemetry processing, and hybrid computing in mind.

Macro instructions which provide control of realtime input-output devices such as multiplexers, A/D and D/A Converters, magnetic tapes and disks, etc., are incorporated. Instructions designed for bit manipulation applications, including PCM data quality checking, will ease the system programmer's job.

FLEXTRAN generates relocatable object code. Separately assembled programs can be linked regardless of the sequence in which the segments or instructions are assembled. This means that several programmers can work on separate sections of a program simultaneously. Input-output devices may be assigned at object time. Object code may be in-line machine code or it may employ subroutines.



RAYTHEON 520 FORTRAN II & IV

Both the language and the processor that make up Raytheon 520 FORTRAN II have been expanded beyond basic FORTRAN to provide the user with a rich procedure-oriented programming system unexcelled in its class.

Major advantages include removal of most of the redundancies and logically unnecessary restrictions of earlier versions of the language. In addition, the meanings of some of the other features of FORTRAN have been generalized so that they apply to more situations than formerly. The result is that Raytheon 520 FORTRAN II language is easier to learn, easier to use without making minor errors, and is more powerful than earlier versions of FORTRAN.

The Raytheon 520 FORTRAN IV System has for its basis the language that is the standard FORTRAN advanced by the American Standards Association. This language has been enhanced by facilities that enable the rapid and efficient development and testing of programs written in FORTRAN. In addition, the language has been enriched to permit exploitation of such machine features as the hardware interrupt facilities, thus providing the basis for real-time capability. The processor also allows programs written in FLEXTRAN to be incorporated in FORTRAN programs.

The Raytheon 520 FORTRAN IV processor is treated simply as another system program that is called and executed under control of the operating system monitor, BOSS. For this reason, the processor is easy to use, providing optimum throughput in both the batch-compile and compile-and-execute modes. Moreover, as an intrinsic part of the programming support package, FORTRAN IV shares with FLEXTRAN the subroutine library commonly structured to satisfy the needs of both.

THE 1620 SIMULATOR

The IBM 1620 Computer was oriented toward "stand-alone" scientific applications. There are approximately 1,500 of these units reported to be in use. For many of these users who wish to move up to a modern, high-speed, system oriented processor, Raytheon provides a 1620 Simulator. It allows use of the thousands of existing machine language programs and can extend the amortization of a large programming investment. Its most important benefit is to provide low-cost, smooth transition to the Raytheon 520 System without the expensive, disruptive process which normally accompanies change over.

The 520 System user who has not replaced a 1620 benefits also. He may utilize the many application programs for the 1620 as they enter the 520 Programming Library. He may also exchange programs with the 1620 computers in his or associated organizations.

All basic and optional 1620-I and II instructions are simulated to allow direct execution of machine language programs. The Raytheon 520, because of its efficient simulation capability, executes 1620 programs at least three times faster than the 1620 Mod I. Programs written in the 1620 FORTRAN source language would, of course, be compiled and executed at much higher speed via 520 FORTRAN, without use of the 1620 Simulator.

The 1620 Simulator provides data processing serially by digit or variable length decimal fields.

IBM 1402 Card Reader/Punch and a Disk Pack are available with the 520 System. Where these peripherals are already available at a 1620 site, Raytheon will interface to them and provide further use of an existing user investment.

THE RAYTHEON 520 INPUT/OUTPUT SYSTEM

The Raytheon 520 provides the most powerful and useful input/output capability available in machines of its class. Input, output and computing can occur simultaneously. Basic input-output character rate is 560KC; word rate is 140KC.

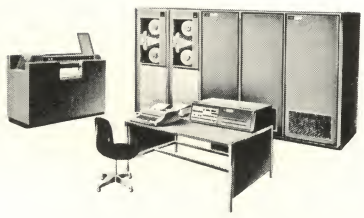
The 520's Input/Output System features the use of a true dual-bus structure (input and output) to which peripheral devices may be added at any time. Direct addressing for up to 512 devices is provided.

Devices are connected to the I/O bus via a controller interface which is unique for each type of device. Each controller has buffer storage appropriate to the device, e.g., 6-bit buffers for paper tape and typewriter I/O and dual 24-bit buffers for magnetic tape. Since there is an individual buffer for each device, it is not necessary to time-share one buffer among many devices. Each of the four I/O channels may be time-multiplexed among many devices, giving the 520 the ability to input, output, and compute simultaneously.

All I/O devices are physically connected to the I/O bus at all times. Under program control, a device may be electronically connected to ("selected") or disconnected from ("deselected") any one of the four 24-bit I/O channels. Each channel is provided with an interrupt line.

PERIPHERAL EQUIPMENT

Typewriter	15 cps
Paper Tape	110 cps punch 300 cps read with rewind, read reverse, and spoolers
Punched Cards	100 cpm reader, 100 cpm punch 800/250 cpm reader punch
Magnetic Tape	45 ips, 75 ips 200 bpi, 556 bpi, 800 bpi 9KC — 120KC
Line Printers	300 lpm, 600 lpm, 1250 lpm 80, 120, 132 or 160 columns
Disk Pack Memory	2 million 6-bit characters per drive, IBM 1311 - compatible (disk file memory also available)
Multidevice Controller	Generalized data system interface allows simple, low-cost expansion by the user with standard sub-assemblies and digital modules
Direct Memory Option	Provides high speed block transfer capability between I/O device and memory with simultaneous computation



MAGNETIC TAPE CONTROLLER

The magnetic tape controller provides two 24-bit buffer registers; one buffer transfers 24-bit parallel words to/from the I/O bus, the other acts an an assembly/disassembly register and transfers 6-bit characters to/from the magnetic tape read/write electronics. The use of dual buffering allows the computer program a maximum of one word time rather than the usual one character time to respond to an interrupt and hence allows more computing during tape operations.

The Raytheon 520 System's programmed magnetic tape format control capability allows maximum flexibility, system efficiency, and computation during tape operation.

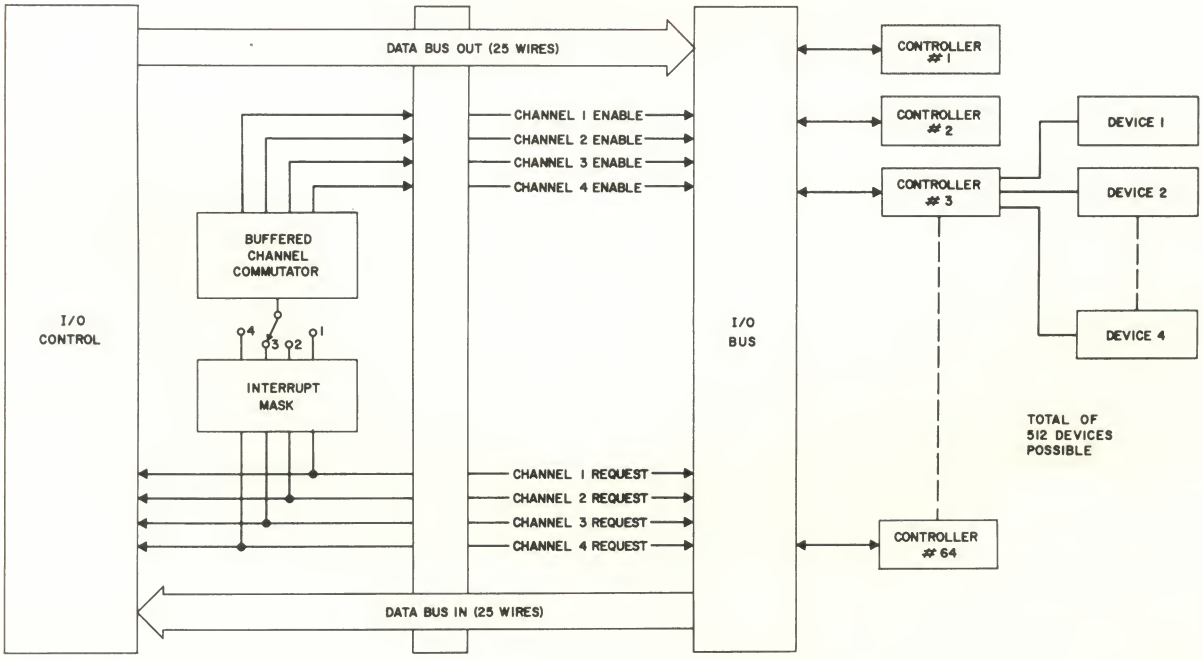
Since input-output format of the tape controller is under program control, the programmer may designate each computer word to contain 1, 2, 3, or 4 characters. This technique avoids the necessity of packing, under program control, four characters per word before an output operation or unpacking during input.

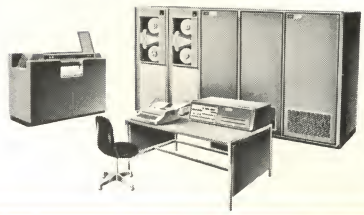
The exceptionally fast code translation and radix conversion capability of the Raytheon 520 System allows efficient communication with a variety of on-line devices without the need for expensive external translation circuitry. This capability is important in working with communication terminals, laboratory instruments, displays and other external data systems devices.

DIRECT MEMORY INPUT/OUTPUT OPTION

High speed data transfers may be handled independently of the central processor by exchanging data directly between the I/O device and memory. This option allows data transfer rates of up to 400,000 words per second.

The address of the starting position in memory and the block length in words are loaded via the central processor into hardware registers contained in the I/O adapter unit. After starting, no further attention from the central pro-





cessor is required until the block transfer has been completed. At this time, at the programmer's option, the central processor may or may not be signaled via the interrupt system. In this manner, for example, data may be entering one area of memory from a disk pack or file while a second area of memory is being unloaded onto magnetic tape and the central processor is computing on unrelated data.

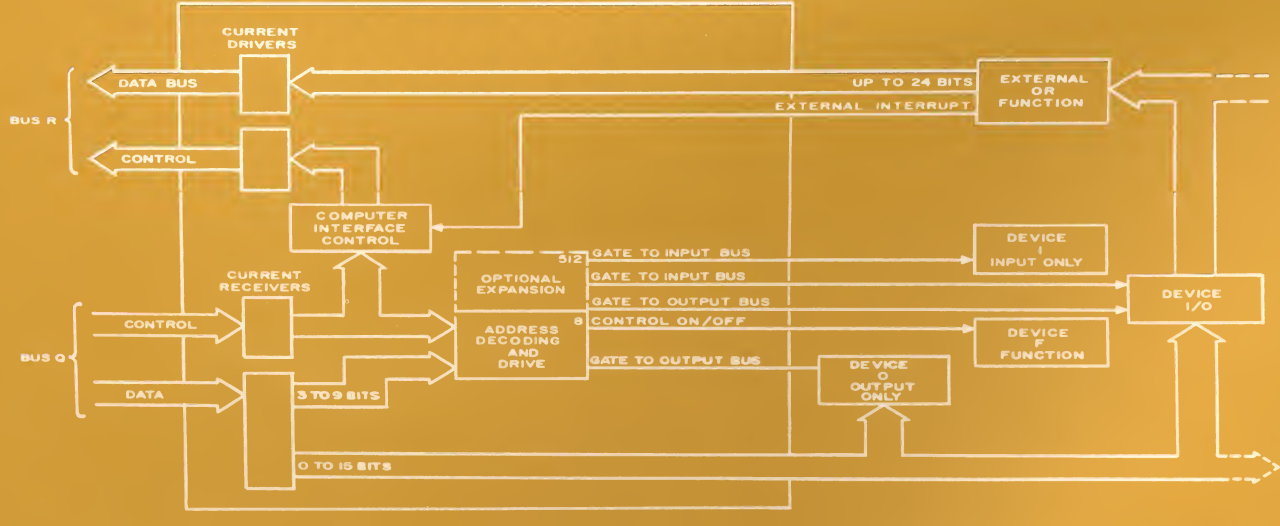
RAYTHEON 520 SYSTEM MULTIDEVICE CONTROLLER (MDC)

Almost all data system requirements are easily and efficiently implemented with the 520's Multidevice Controller. This unit serves as an interface between the 520's I/O bus and up to 512 external data systems devices.

The MDC provides a 24-bit input data bus, a 15-bit output data bus, and a 9-bit address bus. Address and output data bus information are output simultaneously as one 24-bit word. External device identity and data are transmitted in a single I/O operation. This takes advantage of the 520's register format and results in more efficient use of memory, computer time and I/O time.

An optional priority interrupt system may be added to the MDC. This features the direct development of a 15-bit address unique for each interrupt level, logic for gating out lower levels so that a given level may be interrupted by a higher level, a mask register that allows each unique level to be enabled or disabled without affecting the other levels.

Many other options are available for the MDC. These include: standard pre-wired module cases to expand the basic unit up to 512 decoded device selection lines; input assembly registers or output disassembly registers that allow packing one 24-bit, two 12-bit, three 8-bit or four 6-bit data words into one computer word; interval timers of 15 or 24 bits with programmable input frequencies; BCD time-of-day digital clock; analog timing subsystem; output control registers; sense switch input control registers, and digital counters.



RAYTHEON 520 SYSTEM APPLICATIONS

GENERAL PURPOSE SCIENTIFIC PROBLEM SOLVING

The Raytheon 520 System has been designed for this application and provides hardware and software capabilities for many configurations. Open shop problem solving on smaller configurations using FLEXTRAN or the 1620 Simulator are appropriate. For a typical small configuration, the 520 processor could be equipped with an 8192 word core memory. For expanded requirements, a system could include a processor with 12K of main memory, a 512 word fast memory, disk pack, magnetic tape, line printer, etc. A typical system is diagramed below. Maximum productivity of a system this size can be achieved by use of the BOSS operating system. An 8192 word core memory with or without the 200 nanosecond fast memory may be employed with typewriter and card or paper tape input-output. The system may be expanded to include disk pack, magnetic tape, line printer, etc., as appropriate.

The 520 System may be interfaced to realtime data acquisition sources or teletypewriter, and can output results for closed loop control or hybrid computation when the user need expands to include these requirements.

DATA ACQUISITION

Raytheon will provide complete data acquisition and data processing systems for applications such as medical experiments, rocket engine tests, meteorological sensors, nuclear experiments, seismic surveys, wind tunnels, oceanographic mapping, or process monitoring.

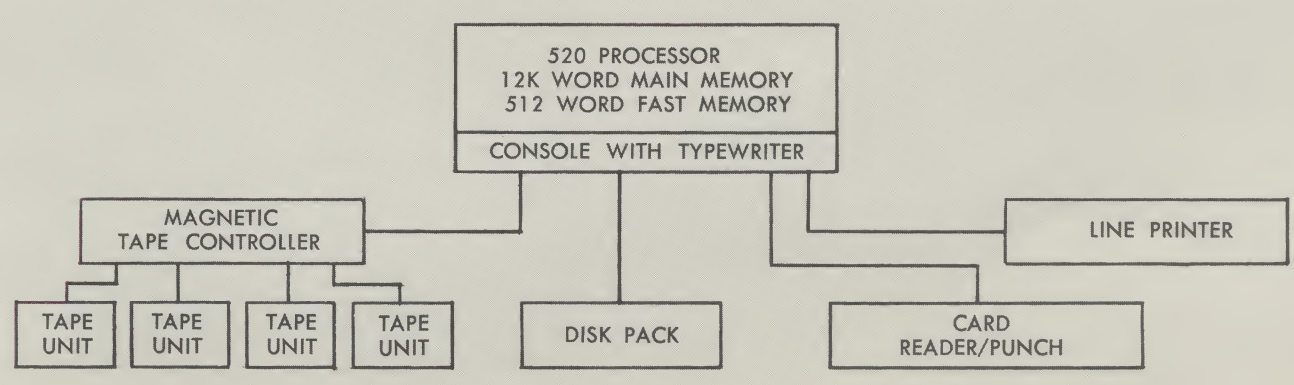
Unique analog instrumentation products and engineering skills assure the customer of a reliable, high performance data system. The Multiverter®, a standard product available only from Raytheon, provides: a 1000 megohm input, 0.01% integrated circuit Multiplexer capable of 250 KC switching; a 50 nanosecond, 0.01% Sample and Hold Amplifier; and anyone of several 0.01% high-speed A/D Converters. These functions, and up to 96 channels of Multiplexer, may be housed in a single self-powered 5¼" high drawer for rack mounting. This data acquisition front end is typically supplied with 15-bit (14-bits plus sign), 30 KC throughput, or 12-bit (11-bit plus sign), 50 KC throughput.

Other data system products, including high-speed 0.01% D/A Converters, are available from Raytheon.

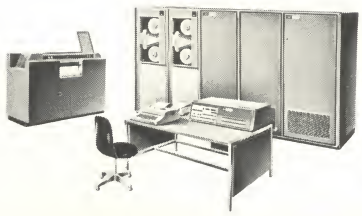
For those situations where 6 or 8-bit A/D conversion is appropriate, Raytheon provides a 5 or 1 MC converter.

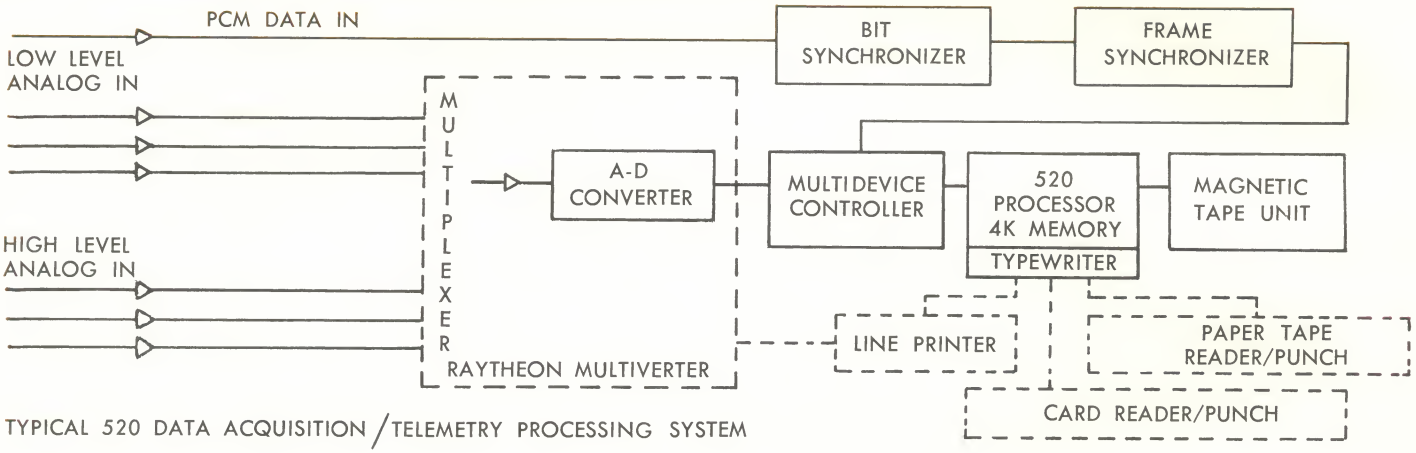
The Raytheon 520 System includes the Multidevice Controller for realtime I/O interface to the processor as described elsewhere in this brochure.

A typical Raytheon 520 System application to data acquisition is shown on the next page.



RAYTHEON 520 SYSTEM TYPICAL SCIENTIFIC CONFIGURATION





TYPICAL 520 DATA ACQUISITION / TELEMETRY PROCESSING SYSTEM

TELEMETRY DATA REDUCTION

Telemetry data acquisition and reduction is another current application in the real-time data systems area where the Raytheon 520 System demonstrates advantages in data throughput rate and flexibility of data manipulation.

A typical system consists of a 520 System plus the peripheral equipment required to accept and process PCM, PAM, and PDM telemetry data, high-level analog inputs and additional serial and parallel digital data.

The capabilities of a Raytheon 520 System in such an application would include:

1) Handling continuous PCM data input, gapped magnetic tape output at 120KC — over 650,000 bits per second with a 40 percent computer duty cycle.
2) Handling continuous digital tape input at 90 KC, output gapped tape at a 120 KC character rate — less than 30 percent computer duty cycle.
3) Providing computer addressing of an optional analog multiplexer and analog-to-digital converter, sampling, conversion (11 bits plus sign), formatting, and writing gapped IBM-compatible tape — 40,000 samples per second.
4) Providing computer addressing of an optional analog multiplexer and analog-to-digital converter, sampling, conversion (11 bits plus sign), formatting, linearizing, and writing gapped IBM-compatible tape — 20,000 samples per second.
5) Performing PCM data decommutation and distribution to digital and analog displays by computer stored program, limit tests, linearization and magnetic tape recording at rates in excess of 250,000 bits/sec.

A similar system is now operational for the Air Force Systems Command at Eglin Air Force Base. Details will be furnished on request.

THE 520 AS A "BLACK BOX"

System engineering organizations will want to consider the 520 for use in custom systems requiring high-speed digital computation, data formatting, communications switching, or digital simulation. Its ultra fast internal speed, including 45 one-microsecond instructions and register-to-register operations, makes it a powerful system component. Two hundred nanosecond memory with register load every microsecond is a unique capability for function generation, table look-up, executive control, data output, etc. 520 I/O is in keeping with high-speed system demands.

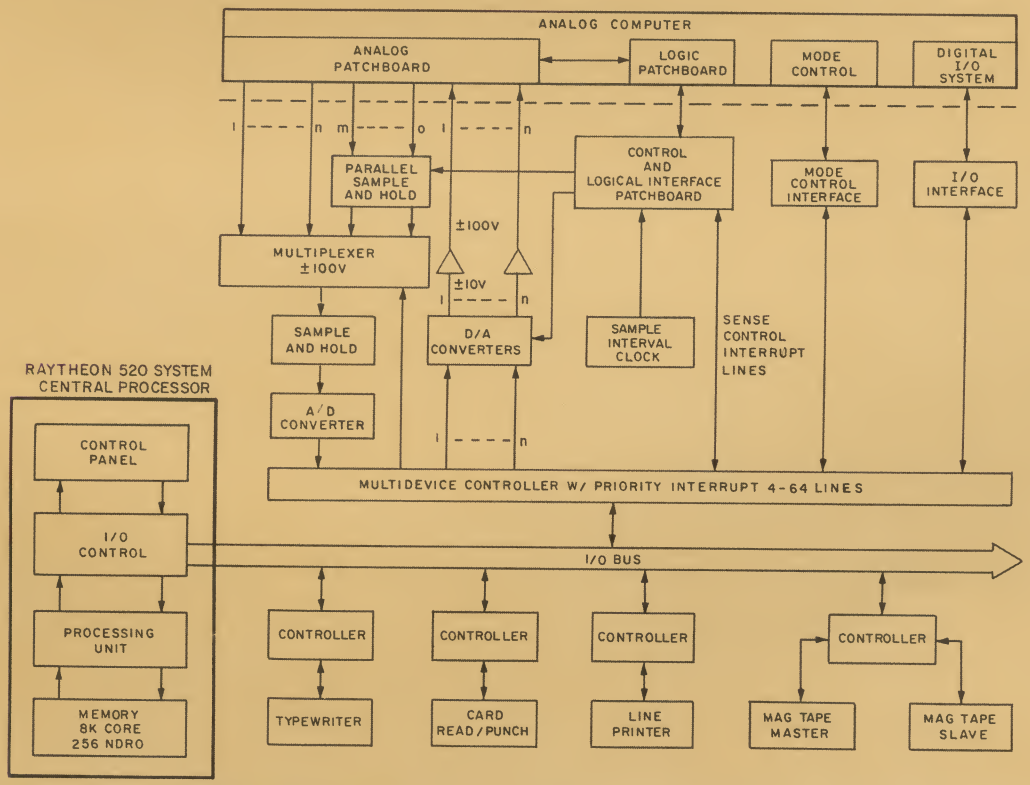
THE RAYTHEON 520 SYSTEM FOR HYBRID COMPUTING – HYCOMP 520

Raytheon Computer has had broad experience in supplying digital computers or linkage subsystems for hybrid analog-digital computing systems. This experience is based on capability in the design, and manufacture and application of digital computers themselves, as well as the analog-to-digital converters, digital-to-analog converters and other equipment and software required for efficient and accurate communication between the two major elements of the system.

The new Raytheon 520 System's high internal processing speeds, especially its high-speed multiply operation, its 1 microsecond register-to-register add and its ability to input/output up to 280,000 12-bit words per second make it well suited for hybrid computing applications. The 520's 200-nanosecond memory allows ultrafast table look-up, function generation and floating point arithmetic operations.

Raytheon is also applying the latest technology to the computer linkage system. A new development—the Multiverter®—introduces integrated circuits to the Raytheon equipment line and makes possible the packaging of 96 channels of 0.01% multiplexing, a 50 nanosecond, 0.01% sample-and-hold amplifier and any one of Raytheon Computer's standard line of high-speed, 0.01% accurate analog-to-digital converters in a single drawer 19 inches wide by 5¼ inches high. This "data system in a box" provides a throughput rate of up to 50KC, significant for hybrid computing applications.

Subroutines which can be called by FORTRAN CALL Statements for system control permit simplified programming of the 520 for hybrid applications.



RAYTHEON 520 HYBRID COMPUTER SYSTEM

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